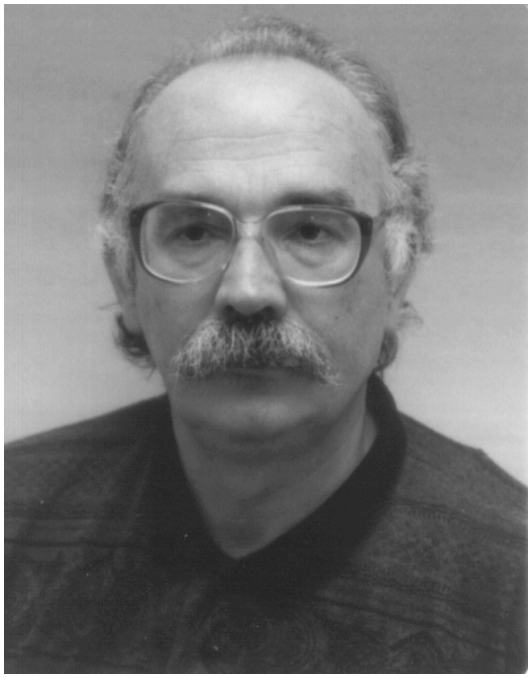

Prof. Vančo B. Litovski

http://leda.elfak.ni.ac.yu

1. Kratka biografija

Prof. Litovski rođen je 1947. god. u s. Rakita, Južna Makedonija, Grčka. Osnovnu i srednju školu učio je u Bitolju. Na Elektronski fakultet u Nišu upisao se 1965. god., a diplomirao je marta 1970. god. Za asistenta na Katedri za Elektroniku Elektronskog fakulteta primljen je 22. marta 1970. god. Magistrirao je juna 1974. god. Vojni rok je odslužio 1974/75. god. Doktorirao je juna 1977. god., a za redovnog profesora Elektronskog Fakulteta u Nišu izabran je 1987. god. Za viziting profesora na Univerzitetu u Soutemptonu izabran je novembra 1999. god. U toku dvanaest godina obavljao je dužnost šefa katedre za Elektroniku Elektronskog Fakulteta u Nišu. Prof. Litovski predaje predmete “Elektronika I“ i “Projektovanje elektronskih kola“. Predavao je i predmete “Fizički osnovi Elektronike” i “Pojačavači”. U školskoj 1999./2000. god. Prof. Litovski je po prvi put na srpskom jeziku održao kurseve iz “Testiranja elektronskih kola” i “Neuronskih mreža”. Kao nastavnik na redovnim ili poslediplomskim studijama bio je angažovan na univerzitetima u Prištini, Sarajevu, Novom Sadu i Banjoj Luci.

U toku svojih stručnih aktivnosti Prof. Litovski bio je više godina angažovan kao savetnik Generalnog direktora Ei za pitanja razvoja.

Prof. Litovski je član “Institute of Electrical and Electronic Engineers“, kao i "Associacion for Computing". Član je predsedništva ETRAN-a.

Prof. Litovski je inicijator i prvi predsednik Jugoslovenskog Društva za Simulaciju, koje je osnovano februara 1999. god.

Prof. Litovski je redovni član Akademije Inženjerskih Nauka Srbije.

Dobitnik je više nagrada Univerziteta u Nišu i Grada Niša za uspeh na redovnim studijama i za doprinos razvoju Elektronskog Fakulteta (Povelju 1980 god., Povelju 1985 god. i Specijalno priznanje 1995 god.) i Univerziteta u Nišu (Plaketa 1985). Dobitnik je “Priznanja” Elektrotehničkog fakulteta u Banjoj Luci za poseban doprinos u razvoju ETFa, kao i “Velike Povelje” Elektrotehničkog Fakulteta u Istočnom Sarajevu “u znak priznanja za višegodišnji savjestan rad ispunjen predanošću i odgovornošću i doprinos razvoju ETFa”. Dobitnik je Povelje časopisa Tehnika povodom dvadesetipet godina izlaženja časopisa kao i “Velike Povelje” ETRANa “u znak priznanja za izuzetan doprinos razvoju naučne i stručne misli u

oblasti Elektronika". Dobitnik je Nagrade ETAN-a za najbolji rad u Komisiji za Elektroniku za 1986. god., kao i Tesline Nagrade za "vrhunska inženjerska tehničko tehnološka ostvarenja" za 1994. god. Jula 1998. god. grupi autora sa Elektronskog Fakulteta, pod vođstvom prof. Litovskog, Evropska Federacija Društava za Simulaciju dodelila je "Savastano nagradu" za najbolji objavljen rad u periodu 1995-1997. god.

U okviru razvoja nastavne infrastrukture i unapređenja nastavnih planova i programa, Prof. Litovski bio je angažovan kao rukovodilac niškog dela u okviru dva TEMPUS projekta (JEP_JEP-17028-2002 i JEP_41107-2006). On je rukovodio i sa Projektom CDP+ N° 20/IS/06, koji je finansirao WUS Austria za Elektrotehnički fakultet u Istočnom Sarajevu.

Prof. Litovski je osnovao i razvio prvi međunarodni naučni časopis iz oblasti Elektronike na Univerzitetu u Nišu: "Facta Universitatis, series: "Electronics and Energetics". Pored toga, prof. Litovski bio je član prve redakcije časopisa "Elektronika" koji je u periodu od pet godina izdavala Elektronska Industrija iz Niša. Kao recenzent redovno je angažovan od strane IEEE CAS, IEE Proceedings, J. of Franklin Institute, Int. J. of Information Technologies i Microelectronics reliability.

Prof. Litovski s ponosom tvrdi da je na Elektronski Fakultet u Nišu doveo računarsku grafiku, UNIX operativni sistem, simulaciju elektronskih kola i sistema, projektovanje integrisanih kola, TCP-IP protokol, superračunarstvo zasnovano na Beowulf tehnologiji, neuronske mreže i jezike za opis hardvera, a prvi je uveo u nastavu NIDAQ-LabView tehnologiju.

Prof. Litovski živi u Nišu, oženjen je i otac je dvoje punoletne dece.

2. Naučna aktivnost

Naučno-istraživački rad Prof. Litovskog vezan je za primenu računara u projektovanju elektronskih kola (diskretnih i integrisanih). Budući jedan od pionira u ovoj istraživačkoj oblasti on je praktično postavio temelje za istraživački kao i obrazovni rad u Srbiji. U najranijoj fazi bavio se razvojem metoda za primenu računara u sintezi i projektovanju električnih i elektronskih telekomunikacionih filtara. U ovoj oblasti je doktorirao, a svoje naučne rezultate je objavio u najeminentnijim američkim časopisima. Za njegovo ime vezuje se klasa električnih frekventnih filatara poznata pod nazivom LSM filtri (od Lest-Squares Monotonic). Krajem sedamdesetih godina započeo je istraživački rad u oblasti projektovanja integrisanih kola. Istraživački rad se odvijao u okviru istraživačke laboratorije za projektovanje elektronskih kola (LEDA) koja je osnovana na Elektronskom Fakultetu na inicijativu i pod rukovodstvom Prof. Litovskog kao prva naučna laboratorija na fakultetu. U toj oblasti najpre su njegovim ličnim radom kao i radom pod njegovim rukovodstvom razvijeni prvi jugoslovenski simulatori elektronskih kola. Ova je oblast istraživanja aktuelna i danas, tako da može da se kaže da je Elektronski fakultet i njegova istraživačka laboratorija LEDA jedna od vodećih istraživačkih organizacija za ovu oblast na svetu. Softeverski paketi za simulaciju elektronskih kola i sistema sa mešovitim signalima (koji omogućavaju simulaciju sistema koji se delimično opisuju parcijalnim, delimično običnim jednačinama, a delimično se ponašaju kao diskretni sistemi), u radu su na više univerziteta širom zapadne Evrope.

Automatizacija projektovanja topologije integrisanih kola je naredna aktivnost koja je negovana u okviru LEDA. Razvijeni su prvi jugoslovenski integrisani softverski paketi za projektovanje integrisanih kola tipa polja gejtova. Ovi paketi našli su direktnu primenu u lokalnoj industriji. Projektovana su integrisana kola tipa polja gejtova u CMOS tehnologiji. Ovi rezultati stvorili su uslove za spoznaju kompleksnosti i značaja ovog stručnog problema u domaćoj industriji i u velikoj meri su uticali na kasnije investicione odluke u oblasti sistema za projektovanja integrisanih i štampanih kola kod nas.

Prof. Litovski je kod nas pokrenuo istraživanja u oblasti testiranja elektronskih kola i projektovanja za testabilnost. Ovo poslednje naročito se odnosi na uvođenje IEEE 1149.1

standarda. Njegovi istraživački rezultati u ovoj oblasti najvećim delom odnose se na uspostavljanju metodologije modelovanja defekata, simulacije defekata i njene primene u okviru sistema za automatsko generisanje testnih signala analognih i digitalnih kola. On je objavio prvu udžbeničku literaturu iz ove oblasti kod nas. U najnovije vreme uveo je nove metode u dijagnostici elektronskih sistema.

Primena neuronskih mreža i veštačke inteligencije u projektovanju integrisanih elektronskih kola je oblast istraživanja u kojoj je LEDA takođe prednjačila. Prvi međunarodni simpozijum o neuronskim mrežama organizovan je novembra 1990. na Elektronskom fakultetu u Nišu. Prof. Litovski je prvi primenio neuronske mreže za modelovanje elektronskih komponenata. Time je otvoren jedan novi koncept primene black-box modelovanja za elektronske komponente i druge sisteme. Ovi rezultati Prof. Litovskog izazvali su znatno interesovanje u naučnoj javnosti. Oni su i danas predmet interesovanja, a o značaju ovih rezultata govori i činjenica da su ova istraživanja u 1999/2000. god. praktično finansirana samo od strane britanskog ministarstva nauke. U ovu oblast istraživanja najvećim delom pripadaju i rezultati prof. Litovskog koji su dobijeni pri generisanju simboličkih funkcija elektronskih kola.

Prof. Litovski je prvi na Elektronski Fakultet doveo istraživanja iz oblasti održivog razvoja. Pri tome naglasak je stavljen na odživo i eko-projektovanje u elektronici što uključuje celokupni životni vek proizvoda. Pored stručnih i naučnih rezultata u ovoj oblasti prof. Litovski je znatno doprineo promociji ove nove naučne discipline.

Za ime Prof. Litovskog vezuje se uvođenje novih tehnologija u naučno-istraživački rad na Elektronskom Fakultetu i Univerzitetu u Nišu kao što je UNIX operativni sistem, računarska grafika, standardni jezik za opis elektronskog hardvera VHDL, računarska mreža i internet protokol, članstvo u EUROPRACTICE-u, CADENCE sistem za projektovanje integrisanih kola i sl.

Kao rezultat rada prof. Litovskog mogu se tretirati i osam doktorata i 21 magistrature koje su realizovane pod njegovim rukovodstvom.

Prof. Litovski objavljivao je radove sa 89 koautora od čega 22 iz inostranstva. Prosečan broj autora po radu bio je oko 2,7.

3. Citiranost

Rezultati Prof. Litovskog citirani su više puta što će ovde biti opisano s tim što će biti izostavljeni *citati LEDA autora uključujući i sopstveno citiranje kao i citiranje od strane njegovih koautora uopšte*.

i) U radu: S. Sadughi, and H.K. Kim, "An approximation procedure for selective linear phase filters", IEEE Trans. on Circuits and Systems, Vol. CAS-34, No. 8, 1987, pp. 967-969, kaže se: "The second example is a filter of order 8 with two finite transmission zeroes and one pair of complex zeroes. It is designed for comparison with the design example given by Litovski [7]. Pod [7] citira se sledeće: V. B.. Litovski, "Synthesis of monotonic passband sharp cutoff filters with constant group delay response", IEEE Trans. on Circuits and Systems, Vol. CAS-26, pp. 579-602, August 1979.

ii) U radu: Topa, M., et all., "*Postprocessing techniques for approximate symbolic network functions of complex analog integrated blocks*", Proc. ECCTD' 97, Budapest, September 1997., pp. 1464-1467, kaže se: "Next it is counted how many times each symbol occurs in a term. This is performed in much the same way as described in [6]", gde je pod [6] citiran rad: Petković, P., Stojilković, S., and Litovski, V., "*Factorization algorithm for symbolic circuits analysis*", IEE Electronic Letters, Vol. 31, No. 13, pp. 1026-1027, June 1995.

iii) U radu: Ževma, A., and Zajc, B., "*Functionality fault model: a basis for technology-specific test generation*", Microelectronics Reliability", Vol. 38, No. 4, pp. 579-604, 1998, kaže se: "Although it is becomming evident that the most accurate fault modelling in digital circuits implemented in CMOS technology is at the transistor level [4-6] the simplicity ....". Pod [4] citiran je rad: Milovanović, D. B., and Litovski, V. M., "*Fault models of CMOS Circuits*", Microelectrinics Reliability, Vol. 34, No. 5, pp. 883-896, 1994.

isti rad se citira i u:

2. Sedaghat, R., Kunchwar, M., Abedi, R., and Javaheri, R., "*Transistor-level to gate-level comprehensive fault synthesis for n-input primitive gates*" Microelectronics and Reliability**,** Volume 46, Issue 12, December 2006, Pages 2149-2158
3. Zemva, A., and Zajc, B., "*Test generation for technology-specific multi-faults based on detectable perturbations*", Microelectronics Reliability, Vol. 45, No. 1, Jan. 2005, pp. 163-173.
4. Ovaj se rad citira u: "Zorian, Y., AT&T Bell Laboratories, Hlavicka, J., Czech Technical university, "*East Meets West*", Guest Editors' Introduction, IEEE Design and Test of Computers, Spring 1996 (Vol. 13, No. 1), pp. 5-7, na sledeći način: D.P. Milovanovic and V.B. Litovski from the University of Nis (Yugoslavia) search for modeling procedures and fault models for BiCMOS circuits. Simulation results analyze fault mechanisms and behavior.
5. Liao, W., Tian, F., and Liu, J., "Efficient fault diagnosis method in nonlinear circuits based on neural network", Computer Engineering and Applications, Vol 45, No.19, 2009, pp. 228-231.

iv) U radu: Senturia, S. D., "*CAD challanges for Microsensors, Microactuators, and Microsystems*", invited paper, Proceedings of the IEEE, Vol. 86, No. 8, August 1998., pp. 1611-1626, citiraju se dva rada prof. Litovskog

1. Mrčarica, Ž, Ilić, T., Glozić, D., Litovski, V., and Detter, H., "*Mechatronic Simulation Using Alecsis: Anatomy of the Simulator*", Proc. of the Eurosim'95, Vienna, Austria, Sept. 1995, pp. 651-656 i
2. Mrčarica, Ž., Litovski, V. and Detter, H., "*Modeling and simulation of microsystems using hardware description language*", Microsystem Technology, Vol. 3, No. 2, 1997, pp. 80-85, pri čemu se, na primer, o drugom kaže: "And using so-called "hardware description languages" [178]-[180], such models can be readily inserted into circuit simulators for behavioral simulation at the system level, including feedback effects around nonlinear devices."

Slično se u knjizi: Pelz, G., *"Mechatronic Systems"* John Wiley & Sons, Ltd, 2003 , Print ISBN: 0470849797 Online ISBN: 0470867906, citiraju radovi:

3. Ž. Mrčarica, Z. Randjelović, M. Jakovljević, V. B. Litovski, H. Detter, "*Methods for description of microelectromechanical device models for system-level simulation*", MICROSIM II, Proc. of the Conf. On Simulation and Design of Microsystems and Microstructures MICROSIM '97, Lausanne, Switzerland, September 1997, pp. 271-280 i
4. Mrčarica, Ž, Ilić, T., Glozić, D., Litovski, V., and Detter, H., "*Mechatronic Simulation Using Alecsis: Anatomy of the Simulator*", Proc. of the Eurosim'95, Vienna, Austria, Sept. 1995, pp. 651-656
5. Mrčarica, Ž., Glozić, D., Litovski, V. and Detter, H., "*Simulation of microsystems using a behavioural hybrid simulator ALECSIS*", International Conference on Simulation and Design of Microsystems and Microstructures (MicroSIM), Vol. 1, 1995, pp. 129–136.

6. Mrčarica, Ž., Litovski, V. B., Delić, N. and Detter, H., "*Modelling of micromechanical devices using hardware description language*", InternationalConference on Micro System Technologies, 1996, pp. 293–298.

v) U specijalnom broju časopisa IEEE Spectrum, posvećenom budućem čipu sa sto miliona tranzistora, autor članka Chappel, B., "*The fine art of IC design*", IEEE Spectrum, Vol. 36, No. 7, July 1999., pp. 30-34, kaže: "For background reading, a textbook that starts at the basics and covers the basic solution methods used in most modern CAD capabilities is *VLSI circuit simulation and optimization* by, V. Litovski and M. Zwolinski ...". Gđa Chappel "is a principal engineer with Intel Corp.'s Tecnology Department within the Microprocessor Products Group in Hilsboro, Ore., where she has been since 1995. For 17 years prior that, she was a member of the research staff at IBM Corp.'s Thomas J. Watson Research Center, Yorktown Heights, N.Y ...".

Isto se citira i u

2. Dreyer, A., "*Interval Methods for Analog Circuits*", Berichte des Fraunhofer ITWM, Nr. 97 (2006) Fraunhofer-Institut für Techno- und Wirtschaftsmathematik ITWM, 2006, ISSN 1434-9973, (prva referenca!) i u
3. Dreyer, A., "Interval Analysis of Linear Analog Circuits", 12th GAMM - IMACS International Symposium on Scientific Computing, Computer Arithmetic and Validated Numerics, 2006. SCAN 2006, Publication Date: 26-29 Sept. 2006, On page(s): 14-14, Location: Duisburg, Germany, ISBN: 978-0-7695-2821-2.

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JULY 1999 VOLUME 36 NUMBER 7

The 100-million transistor IC Design Fabrication

To probe further

For background reading, a textbook that starts at the basics and covers the basic solution methods used in most modern CAD capabilities is *VLSI Circuit Simulation and Optimization*, by **V. Litovski** and **M. Zwolinski** (Kluwer Academic, Dordrecht, the Netherlands, 1997).

About the author

Barbara Chappell is a principal engineer with Intel Corp.'s Design Technology Department within the Microprocessor Products Group in Hillsboro, Ore., where she has been since 1995. For 17 years prior to that, she was a member of the research staff at IBM Corp.'s Thomas J. Watson Research Center, Yorktown Heights, N.Y. Chappell has produced more than 24 publications and has been issued more than 18 U.S. patents.

The fine art of IC design

BARBARA CHAPPELL
Intel Corp.

vi) TECHNION (Israel Institute of Technology, Haifa, Israel) na "Computer Science Department", na predmetu "Algorithmic Aspects in VLSI Design (CS 236604)" koji vodi Dr. Israel Wagner, kao obaveznu literaturu navodi: "*VLSI sircuit simulation and Optimization*", Litovski, V. and Zvolinski, M. (*http://www.cs.technion.ac.il/~wagner/pub/aav.html).*

vii) Technische Universitaet Hamburg-Harburg (TUHH) na odseku "Arbeitsbereit Mikrosystemtechnik", u okviru specijalizacije "Simulation in der Mikrosystemtechnik", u poglavlju "5. System simulation" pratećeg udžbenika *http://www.tu-harburg.de/mst/* kaže: "Subsequently, the operation and algorithmic framework of analog simulation is represented, oriented on the widespread network simulator SPICE [8, 11]. The fundamental techniques can be transferred to most analog simulators". Referenca je: [8] Litovski, V., Zwolinski, M.: *VLSI Circuit Simulation and Optimization*. Chapman and Hall, London, 1997.

viii) National University of Ireland, Galway, u programu za predmet: "VHDL for: ASIC design capture, verification and synthesis", u okviru sekcije booklist, preporučuje: Litovski, V., Zwolinski, M.: *VLSI Circuit Simulation and Optimization*. Chapman and Hall, London, 1997. (*http://www.ee.nuigalway.ie*).

ix) Tehnički Univerzitet u Kilu, Nemačka, na katedri za "Algemeine und Teoretische Electrotechnik" u okviru programa za predmet "Praktikum Schaltungsimulation", Prof. Neumann, I, et. all., Preporučuju u literaturi: Litovski, V.; Zwolinski, M.: *VLSI Circuit Simulation and Optimization*. Chapman and Hall, London, 1997. Slično stoji na: *www.ife.tugraz.at/Elektronik/ Roehrer/Simulation/math.pdf*, tehninčkog Univerziteta u Graz-u, za predmet "Die matematische Methoden in SPICE".

x) Univerzitet u Southamptonu, Engleska, U okviru predmeta Design Automation, Prof. A. Brown, preporučuje: Litovski, V., Zwolinski, M.: *VLSI Circuit Simulation and Optimization*. Chapman and Hall, London, 1997. (*https://secure.ecs.soton.ac.uk/ug/handbook/99/ Units/el325.html*).

xi) Swarthmore College, Velika Britanija, Prof. Erik Cheever, napisao je udžbenik koji je smestio na WEB. U poglavlju "An Algorithm for Modified Nodal Analysis" napisao je: "Many of the ideas and notations from this page are from Litovski, thought the discussion here is quite simpler because only independent voltage and current sources are considered". Govori se o: Litovski, V., Zwolinski, M.: *VLSI Circuit Simulation and Optimization*. Chapman and Hall, London, 1997. (*http://www.swarthmore.edu/NatSci/echeeve1/Ref/mna/ MNA3.html*).

xii) Univerzitet u Linkepingu, Švedska, Otsek za Fiziku, Tehnolgiju merenja, Biologiju i Hemiju, na poslediplomskim studijama realizuje nastavu iz automatizacije projektovanja u elektronici za projektovanje u fizici. U okviru kursa, a za predmet Logička simulacija, preporučuje se članak: Maksimović, D., and Litovski, V., "*Tuning logic simulator for timing simulation*", Electronic Letters, Vol. 35, No. 10. May 1999, p. 800-802. (*http://www.ifm. liu.se/čperla/EDA_Course/ topics.html).*

2. Hochschule für Technik und Wirtschaft des Saarlands, Goebenstraße 40, 66117 Saarbrücken, u nastavnom planu stoji: Modulbeschreibung: Titel des Moduls: Schaltungssimulation und Optimierung, Literatur: Litovski, V.; Zwolinski, M.: *VLSI Circuit Simulation and Optimization*; Chapman & Hall;1997.
3. Slično, National Institute of Technology, Karnataka, Surathkal, Indija, u okviru predmeta:" Modeling and Simulation (3-0-0) 3", na: Department of Electronics & Communication Engineering, preporučuje kao osnovnu literaturu "*Litovski V.,VLSI Circuit simulation and optimization*", Chapman & Hall, 1997, ISBN 0-412-63860-6

4. Manchester Metropolitan University, Faculty of Science and Engineering, Department of Engineering, u nastavnom planu stoji: Postgraduate Network in Advanced, Subject area: H610 Electronic Engineering, Unit title: Electronic Circuit Design, Unit code number: 64ET4505, Unit leader(s) Mr. L.Travis, Dr. F.J.Swift, Indicative student learning resources: "*Litovski V.,VLSI Circuit simulation and optimization*", Chapman & Hall, 1997, ISBN 0-412-63860-6

5. Technische Universitaet Graz, Institut fuer Elektronik, u nastavnom planu stoji: Lehrversnstaltungen, Schaltungssimulation, Matematische metoden in der Schaltungssimulation, SSIM VO. 2005, ...Referenzen, [3] Litovski, V.; Zwolinski, M.: VLSI Circuit Simulation and Optimization; Chapman & Hall;1997.
http://www.ife.tugraz.at/Elektronik/Soeser/Simulation/SSIM_mathematische_Methoden.pdf

xvi) Ecole Nationale Supérieure des Télécommunications, Département COMELEC , Prof. Hervé Petit, za kurs: "*Introduction à la simulation électrique* " preporučuje: [1] C.W. Ho, A.E. Ruehli et A. Brennan : The Modified Nodal Approach to Network Analysis. *IEEE Transactions on circuits and systems*, juin 1975. [2] V. Litovski et M. Zwolinski : *Circuit Simulation and Optimisation*. Chapman & Hall, 1997. [3] J-P. Nougier : *Méthodes de calcul numérique*. Hermes, 2001. [4] SPICE, http://bwrc.eecs.berkeley.edu/Classes/IcBook/SPICE/.

2. ista se knjiga preporučuje na "Metropolitan University (MU) at Sylhet, Bangladesh", za "B.Sc. Engineering in Electronics & Telecommunication Engineering (ETE)" kao literatura za predmet "Very Large Scale Integration (VLSI)".
3. kao i na "National Institute of Technology, Karnataka, Surathal,, India" na "Division of Electrical, Electronics, and Computing Systems", pri "Depat. Of Electronics and Communication Engineering",za predmet "Modeling and simulation".

xvii) ESTIA: Ecole Superieure des Technologies Industrielles Avancees, (64102 Bayonne Cedex, France) u prijavi doktorske teze Frederic-a Seyler-a čiji je naslov: "*Conception et prototypage d'un simulateur de circuit electrique a partir du schema de principe du circuit (extensible aux circuit hydrauliques et pneumatiques)*", kao prva bibliografska jedinica navodi se: "*VLSI sircuit simulation and Optimization*", Litovski, V. and Zvolinski, M.. (*http://www.estia.fr/čncouture/last_sujet.html*). (*http://dept-info.labri.u-bordeaux.fr/~maylis/DEA/sujet1.html*).

Ista se referenca citira i u magistarskoj tezi:

2. Li Zheng,"*A Distributed Environment for the Simplification of Multiple Boolean Functions*", The University of East Anglia, Norwich, Engleska, Oktobra 1997. *http://www. itr.unisa.edu.au/člzheng/MSC_Li.pdf*,
3. i u magistarskoj tezi: Lakshminarayanan, C. C., "*An Analog kernel using direct method for solving ordinary differential-algebraic equations in a Mixed-mode Simulator*", University of Sinsinnati, Deparment of Electrical and Computer Engineering and Computer Science of College of Engineering, USA, December 1997.
4. i u doktorskoj disertaciji: Ingo Naumann, "Sortierverfahren und Datenstrukturen in der VLSI-Netzwerksimulation", Technischen Fakult¨at der Christian-Albrechts-Universit¨at zu Kiel, Kiel 2003.
5. i u doktorskoj disertaciji: Chen-Wei Liu, *"Floorplan and Power/Ground Network Co-Synthesis for Fast Design Convergence*", Graduate Institute of Electronic Engineering, National Taiwan University, 2005.
6. i u doktorskoj disertaciji: Chandankumar Reddy Karrem, "Trust-tech based methods for optimization and learning", Faculty of the Graduate School of Cornell University, USA, May 2007
7. u radu: Chen-Wei Liu (Synopsys Taiwan Limited) and Yao-Wen Chang "*Floorplan and Power/Ground Network Co-Synthesis for Fast Design Convergence*", International Symposium on Physical Design, ISPD'06, April 9–12, 2006, San Jose, California, USA.
8. i u radu: Liu, C.-W., and Chang, Y.-W., " Power/Ground Network and Floorplan Cosynthesis for Fast Design Convergence", IEEE Transactions On Computer-Aided Design Of Integrated Circuits And Systems, VOL. 26, NO. 4, APRIL 2007, pp. 693-704.
9. i u doktorskoj disertaciji: Albustani, H., "*Modelling Methods for Testability Analysis of Analog Integrated Circuits Based on Pole-Zero Analysis*", Der Fakultät für Ingenieurwissenschaften der Universität Duisburg-Essen zur Erlangung des akademischen Grades eines Doktor-Ingenieur (Dr.-Ing.) vorgelegte Dissertation.

Referent: Prof. Dr.-Ing. Axel Hunger, Korreferent: Prof. Dr-.Ing. Bernd Straube, Tag der mündlichen Prüfung: 06 August 2004

10. Takođe, i u doktorskoj disertaciji: Sung-Hwan Min, "Automated Construction of Macromodels from Frequency Data for Simulation of Distributed Interconnect Networks", na: School of Electrical and Computer Engineering, Georgia Institute of Technology, April 2004.

Referenca: Litovski, V. and Zvolinski, "*VLSI sircuit simulation and Optimization*", Chapman and Hall, London, 1997, citira se i u radovima (reference, [LiZ 97] [8] i [9], respektivno):

11. -J. Haase (Fraunhofer-Institut für Integrierte Schaltungen, Außenstelle EAS Dresden), W. Vermeiren, Clauss, C., und P. Schwarz, "*Erste Erfahrungen mit der simulation von Mixed-Signal-Schaltungen mit einem VHDL-AMS-Simulator*", ASIM-Tagung, Simulationstechnik, Weimar, 17.09. 1999, Praxisforum, pp. 33-38.
12. -J. Haase, P. Schwarz, P.Trappe und W. Vermeiren, "*Erfahrungen mit VHDL-AMS*", HDL-Workscop, Jena, 25. 11.1999, pp. 29-34.
13. -J. Haase, P. Schwarz, P.Trappe und W. Vermeiren, "*Erfahrungen mit VHDL-AMS bei der Simulation heterogener Systeme*", ITG/GI/GMM Workshop, "Methoden und beschreibungssprachen zur modellirung und verifikation von Schaltungen und Systemen", Frankfurt/M, 28-29.02.2000, pp. 167-175, gde se kaže: "Bei der beschreibung analog-digitaler Teilsysteme ist der definierte mixed-mode-Simulationszyklus zu berueksichtigen [9].
14. i u: Rafael López-Ahumada and Rafael Rodríguez-Macías, "*A Strategy for Rapid Mismatch Evaluation of Transient Characteristics of CMOS Analog Cells*", Analog Integrated Circuits and Signal Processing, Kluwer, Volume 37 , Issue 2 (November 2003) pp. 103 - 111, 2003, ISSN:0925-1030 i
15. i u: Chen, T.-H., Tsai, J.-L., Chen, C. C.-P., Karnik, T., "*HiSIM: Hierarchical Interconnect-Centric Circuit Simulator"*, Proc. of the IEEE ICCAD 2004, November 2004.
16. i u: Shwehdi, M. H., et all., "*A parametric sensitivity formulation for power system analysis*", Proc. of the 14th Power systems computation conference", 14th PSCC, Sevilla, 24-28, June 2002, Session 09, Paper 1, Page 1-7,
17. i u: Brown, A.D., Ross, J.N., and Nichols, K.G. "*Time-domain simulation of mixed nonlinear magnetic and electronic systems*", IEEE Trans. on Magnetics**,** Volume: 37, Issue: 1, Part 2, On page(s): 522-532, Jan 2001, ISSN: 0018-9464.
18. i u: Y.-W. Chang, T.-C. Chen, and H.-Y. Chen, "Physical Design for System-On-a-Chip" in Essential Issues in SOC Design (Y.-L. Lin, Editor), Springer, pp. 311-403, 2006 (invited article).
19. i u: Kato, S. Hoshi, N. Oguchi, K., "*Analysis of power electronics systems including cascaded induction machines with modified nodal analysis*", Proceedings of the Power Conversion Conference, 2002. PCC Osaka, Japan, Volume: 1, pp: 282-287, ISBN: 0-7803-7156-9. Kaže se: "In the modified nodal analysis method, matrix stamps [5] can easily compose the matrix equations used for obtaining solutions.. "
20. i u radu: Damper, R.I., French, R.L.B., and Scutt, T.W., "The Hi-noon neural simulator and its applications", Microelectronics Reliability, Vol. 41, pp. 2061-2065, 2001.
21. i u radu: Blaabjerg, F., Chiarantoni, E., Del L'Aquila, A., Liserre, M., and Vergura, S., "*Sensitivity analysis of an lcl-filter-based three-phase active rectifier via a "virtual circuit" approach*", Journal of Circuits, Systems, and Computers (World Scientic Publishing Company), Vol. 13, No. 4, 2004, pp. 665-686.

22. i u radu: Kato, S., Hoshi, N., Oguchi, K., "*Brushless slip-power recovery system simulation using modified nodal approach*", IEEJ Trans. IA, Vol. 124, No. 12, 2004, pp. 1252-1260.
23. i u: Naumann, I., and Dirks, H.K., "*Efficient reordering for direct methods in analog circuit simulation*", Electrical Engineering ,Volume 89, Issue 4, March 2007, Pages 333-337 **.**
24. i uradu : Cheever, E., "*Demystifying spice: Generating and solving circuit equations symbolically*", Computers in Education Journal, Volume 14, Issue 1, January 2004, Pages 30-37.
25. i u radu: Wan, B., Richard Shi, C.-J.**, "** *Hierarchical multi-dimensional table lookup for model compiler based circuit simulation*", Proceedings - Design, Automation and Test in Europe Conference and Exhibition , Volume 2, 2004, Pages 1310-1315**.**
26. i uradu: Sun, W., Chen, R.M.M., Jiang, Y.-L., "*Tolerance analysis for electronic circuit design using the method of moments*", Proceedings - IEEE International Symposium on Circuits and Systems, Volume 1, 2002, Pages I/565-I/568**.**
27. i u radu: Legrand, F., et all., "*Simul'Elec, a Delphi written simulator for power Electrical Engineering, using VHDL-AMS modeling*", IEEE International Behavioral Modeling and Simulation Workshop, 2007. BMAS 2007., Publication Date: 20-21 Sept. 2007, On page(s): 94-99, Location: San Jose, CA, USA, ISBN: 978-1-4244-1567-0
28. kao i u knjizi Chang, Y.-W., Chen, T.-C., and Chen, H.-Y., "*Physical Design for System-On-a-Chip*", http://cc.ee.ntu.edu.tw/~ywchang/Courses/PD/socpd-fig.pdf.
29. i u knjizi: Frevert, R, Haase, J., Jancke, R., Knoechel, U., (Fraunhofer Institute for Integrated circuits, Dresden, Germany), and Kakerow, R., and Darianian, M., (Nokia reserch center, Bochum, Germany), "*Modeling and simulation for RF design*, Published by Springer P.O. Box 17, 3300 AA Dordrecht, The Nederlands, ISBN 10 0 - 387-27584-3(HB), 2005.
30. U radu: Streibl, M. , Zängl, F., Esmark, K., Schwencker, R., Stadler, W., Gossner, H., Drüen, S., and Schmitt-Landsiedel, D., "*High abstraction level permutational ESD concept analysis*", Microelectronics Reliability, Vol. 45, 2005, pp. 313–321.
31. u habilitacionom radu: Hedrich, L., "Entwurf integrierten analoger schaltungen mit Hilfe symbolischer Methoden", Universitaet Hannover, Hannover, 2004.
32. u: Chalup, S.K., Mellor, D., and Rosamond, F., "*The Machine Intelligence Hex Project*", School of Electrical Engineering and Computer Science, The University of Newcastle, Australia, Technical Report, 21. June 2005. Kaže se: „below we briefly outline the procedure, however anyone considering implementing this approach would be advised to consult a relevant book on circuit simulation, such as that by Litovski and Zwolinski (1997)."
http://www.cs.newcastle.edu.au/~chalup/papers/MIHex2005_tr.pdf.
33. u knjizi: Kahl, K., Edelkamp, K. and Hildebrand, L., "*Learning How to Play Hex*", Book Chapter in: J. Hertzberg, M. Beetz, and R. Englert (Eds.):*"KI 2007: Advances in Artificial Intelligence"*, LNAI 4667, ISBN 978-3-540-74564-8 pp. 382–396, 2007, Springer-Verlag Berlin Heidelberg
34. i u radu: Dong, W., Li, P., and Ye, X., "*WavePipe: Parallel Transient Simulation of Analog and Digital Circuits on Multi-Core Shared-Memory Machines*", 45th DAC, Anaheim, June 2008. http://www.dac.com/45th/PDFs/14.1_BEST_Paper.pdf,
35. i u poglavlju: McPherson, D.S. and Chrisostomidis, C.E., "*CAD techniques*", u knjizi: Robertson I.D., and Rocyszyn, S., "*RFIC and NINIC design and technology*", IEE Circuits, devices, and systems series 13, IEE 2001. (Prva referenca).

36. U radu: Mistrı´k,P., Mullaley, C., Mammano, F., and Ashmore, J., "*Three-dimensional current flow in a large-scale model of the cochlea and the mechanism of amplification of sound*", Journal of the Royal Socociety Interface, Vol. 32, No. 6, 2009, 279–291. Kaže se: "To determine the pattern of current flow within the cochlear equivalent electrical circuit (figure 1*c*), we developed the solution techniques based on MNA (Litovski & Zwolinski 1997) and modified from SCAM (developed by E. Cheever; http://www.swarthmore. edu/NatSci /echeeve1/). MNA allows elements and their connectivities within a circuit of arbitrary complexity to be written down as a table and then to be mapped into a connectivity matrix."
37. u knjizi: Lattarulo, F., "*Electromagnetic compatibility in power systems*", Elsevier, 2007, ISBN 0080452612, 9780080452616.
38. u doktorskim disertacijama:
Legrand, F., "*Modélisation de circuits électrotechniques en vue de leur simulation - Réalisation d'un simulateur*", L'Université Bordeaux I, École doctorale des sciences physiques et de l'ingénieur, 29 janvier 2004.
39. Subramanian, S., "*A Super nodal approach to the linear analog solver in a VHDL-AMS system*", The Division of Graduate Studies and Research Of The University Of Cincinnati, Department of Electrical and Computer Engineering and Computer Science of The College of Engineering, October 22nd 2003.
40. Bounceur, A., « *Plateforme CAO pour le test de circuits mixtes* », Institut national polytechnique de Grenoble, École Doctorale d'Électronique, d'Électrotechnique, d'Automatique et de Traitement du Signal, Grenoble, France, 2007.
41 Rasmussen, R.K., "*Algorithmic approach for plazing and solving shannon games*", The Faculty of Information Technology at The Queensland Universitz of Technology, Brisbane, Australia, 2007.
42. U magistarskim tezama :
Frazier, N., "*Modeling frequency variations in ring oscillators with respect to process parameter variations*", The Graduate Faculty of Texas Tech. University, Decembar 2002.
43. Raghuram, R., "*Improving Simulation Time using Multithreading In Frequency Extended VHDL-AMS*", Master Thesis, Division of Graduate Studies and Research of the University of Cincinnati in the Department of Electrical and Computer Engineering and Computer Science of The College of Engineering, 2002.
44. U knjizi: Hurst, S. , "*VLSI Custom Microelectronics: Digital: Analog, and Mixed-Signal*", Publisher: CRC, November 5, 1998, ISBN-10: 0824702204, ISBN-13: 978-0824702205
45. U nastavnom programu: Course Information – 2009/2010, ECX5231- Network Theory, Department of Electrical & Computer Engineering, Faculty of Engineering Technology, The Open University of Sri Lanka, Nawala, Nugegoda 10250.
46. U knjizi: Graeb, H., "*Analog Design Centering and Sizing*", Springer, 2007, ISBN 1402060033, 9781402060038
47. U radu: Hsin-Hua Pan, Hung-Ming Chen, Chia-Yi Chang, "*Buffer/flip-flop block planning for power-integrity-driven floorplanning*," 10th International Symposium on Quality of Electronic Design, ISQED 2009, SAN JOSE, California, pp.488-493.
48. U radu: Mistrik, P., and Ashmore, J., "Using large scale computational model to study the effect of longitudinal and radial electrical coupling in the cochlea", Proceedings of the 10th International Workshop on the Mechanics of Hearing, CONCEPTS AND CHALLENGES IN THE BIOPHYSICS OF HEARING, Keele University, Staffordshire, UK, 27 – 31 July 2008, edited by Nigel P Cooper (Keele University, UK) & David T Kemp (University College London, UK, pp. 377-383

49. U doktorskoj disertaciji: Ali, S.H.Md, “System level performance and yield optimization for analog integrated circuits”, University of Southampton, Faculty of Engineering Science and Mathematics, Scool of Electronics and Computer Science, 2009.
50. U radu: Chuang, Y.-L., , Lee, P.-W., and Chang, Y.-W., “Voltage-drop aware analytical placement by global power spreading for mixed-size circuit designs”, Proceedings of the 2009 International Conference on Computer-Aided Design, San Jose, California, 2009, ISBN:978-1-60558-800-1, pp. 666-673 i
51. U radu: Hsu, Y.-C., Hsieh, M.F., McMahon, R.A., “A General Design Method for Electric Machines Using Magnetic Circuit ModelConsidering the Flux Saturation Problem”, Proc. of the Eighth International Conference on Power Electronics and Drive Systems, IEEE PEDS2009, November 2-5, 2009, Taipei, Taiwan, R.O.C, pp. 625-630 i
52. U patentu: Chen, H., “S-Matrix technique for circuit simulation”, Pat. No. US 7,660,708 B2, 09 February, 2010.

xviii) Kompanija Hamster, koja sebe predstavlja kao prvi nezavisni proizvodjač VHDL-AMS simulatora za personalne računare, na svom sajtu *http://www. hamster-ams.com/literature.htm*, kao referencu za modelovanje i simulaciju navodi “*VLSI sircuit simulation and Optimization*”, Litovski, V. and Zvolinski, M.

xix) Univerzitet u Bordou, Otsek za informatiku, u prijavi projekta: “*Visualisation en Schematique Electrique*”, kao prvu bibliografsku jedinicu navodi: “*VLSI sircuit simulation and Optimization*”, Litovski, V. and Zvolinski, M. *http://www.dept-info.labri.u-bordeaux.fr/maylis/DEA/sujet. html.*

xx) Tehnički univerzitet u Beču, u prijavi projekta: “*Handhabung und Montage mikromechanischer Bauelemente*”, koji je vodio Dr. Brenner, u spisku važnijih publikacija naveden je rad: Radjenović-Mrčarica, J., Mrčarica, Ž., Detter, H., Brenner, W., and Litovski, V., “*Neural Network Visual Recognition Applied to Microelectromechanical part Assembly*”, VDE Verlag Berlin und Offenbach London, 1996, pp. 325-328. h*ttp://www.tuwien.ac.at/ histu/inst/fp/ 0003580107.html.*

xxi) Tehnički Univerzitet u Beču, 1997 god., u izveštaju po projektu: “*UNICHIP Vienna - ASIC Design with Austrian Universities*”, kao prvi rad navodi: Kero, N., Janković, S., Fallman, W., and Litovski, V., “*A High Speed Serial Bus Controller ASIC*”, Proceedings of MIEL’97, Niš, Yugoslavia, 1997, pp. 737-742. *http://www. iaae. tuwien.ac.at/gme/jb97/97_59.htm.*

xxii) U radu: Gerlach, G., Schroth, A., und Klein, A., “*Modellirung nichtelektrischer Komponenten in heterogenen und komplexen Mikrosystemen*”, Workshop: Methoden und Werkzeuge zum Entwurf von Microsystemen, Frankfut a.M., Juni 1996, pp. 12-21, kaže se: “Die partielle DGL wird ein System gewoenlicher DGL ueberfuert (z.B. durch einen Finite-Differenzen-Ansatz) und direct als Syntax in den Systemsimulator eingegeben [14]. Refernca koja se citira je

1. ”Mrčarica,Ž., Glozić,D., Litovski,V., Detter,H., *"Simulation Of Microsystems Using A Behavioural Hybrid Simulator Alecsis"*, u: Adey, R.A., Lahrmann, A., Lemboe Ilmann, C., editors, “*Simulation and Design of Microsystems and Microstructures*” , Computational Mechanics Publication, Transactions on the Built Environment, Vol 12, © 1995 WIT Press, www.witpress.com, ISSN 1743-3509, Southampton, GB, 1995.

Na istom workshopu, ovaj rad je citiran još dva puta i to u:

2. Klein, A., and Gerlach, G., "*Modeling of piezoelectric bimorph structures using an analog hardware description language*", pp. 229-238, i

3. Bielefeld, J., Pelz, G., and Zimmer, G., "*Electrical network formulation of mechanical finite-element models*", pp. 239-247.

Isti rad je citiran i u

4. Bielefeld, J., Pelz, G., and Zimmer, G.,¨*AHDL-model of a 2D mechanical finite-element usable for micro-electro-mechanical-systems*¨, Proc. of the IEEE/VIUF workshop on behavioral modeling and simulation, 1977, pp. 177-181.

xxiii) U doktorskoj disertaciji: M. Jakovljević, "*System-level modeling of microsystems*", odbranjenoj na Tehničkom Univerzitetu u Beču, 2000 god. citirani su pet radova i jedna knjiga i to:

1. Ž. Mrčarica, V. B. Litovski, M. Jakovljević, H. Detter, "*Hierarchical modelling of microsystems in an object-oriented HDL*", Proc. of the 21st Int. Conf. On Microelectronics, MIEL'97, Niš, Yugoslavia, September 1997, pp. 475-478.

2. Ž. Mrčarica, Z. Randjelović, M. Jakovljević, V. B. Litovski, H. Detter, "*Methods for description of microelectromechanical device models for system-level simulation*", MICROSIM II, Proc. of the Conf. On Simulation and Design of Microsystems and Microstructures MICROSIM '97, Lausanne, Switzerland, September 1997, pp. 271-280.

3. S. Janković, D. Maksimović, P. Petković, and V. Litovski, "*Testable design of Digital ASIC with embedded analog multiplexers*", Proc. of MIEL'97, Niš, Yugoslavia, 1997, pp/. 779-782.

4. Ž. Mrčarica, V. Risojević, M. Lenczner, M. Jakovljević, and V. Litovski, "An *Integrated simulator for MEMS using FEM implementation in AHDL and frontal solver for large-sparse system of equations*", Proc. of Design and Test of Microsystems 99, Paris, March, pp. 271-278.

5. M. Jakovljević, Ž. Mrčarica, P.A. Fotiu, H. Detter, and V. Litovski, "*Analogue behavioural simulator as a tool for coupled electro-thermal analysis of microsystems*", Proc. of MIEL 2000.

6. Litovski, V., and Zvolinski, "*VLSI sircuit simulation and Optimization*", Chapman and Hall, London, 1997.

U dok. diserataciji: Voßkämper, L. M., , "Kohärente Layoutsynthese und Modellbildung von skalierbaren mikroelektromechanischen Strukturen", na: Gerhard-Mercator-Universität, Duisburg, odbranjena 24. Januara 2003, *deposit.ddb.de/cgi-bin/dokserv?idn=96653767x&dok_var=d1&dok_ext=pdf&filename=96653767x.pdf,*

citiraju se radovi :

1. Mrčarica, Z., Glozić, D., Litovski, V., and Detter, H.: "*Simulation of Microsystems using a Behavioural Hybrid Simulator ALECSIS*", International Conference on Simulation and Design of Microsystems and Microstructures (MicroSIM) 1 (1995) 129-136

2. Mrčarica, Z., Litovski, V.B., Delić, N., and Detter, H.: "*Modelling of Micromechanical Devices Using Hardware Description Language*", International Conference on Micro Electro, Opto, Mechanic Systems and Components 5 (1996) 293-298

3. Mrčarica, Z., Ranđelović, Z., Jakovljević, M., Litovski, V.B., and Detter, H.: "*Methods for Description of Microelectro-Mechanical Device Models for System-Level Simulation*", International Conference on Simulation and Design of Microsystems and Microstructures (MicroSIM) 2 (1997) 271-280.

U dok. disertaciji: Luedecke, A., "Simulationsgestuetzte Verfahren fuer den Top-Down Entwurf heterogener Systeme", Universitaet Duisburg, Essen, Nemačka, Decembar 2003, citira se:

1. Mrčarica, Ž., Litovski, V.B., Delić, N., and Detter, H.: "*Modelling of Micromechanical Devices Using Hardware Description Language*", International Conference on Micro Electro, Opto, Mechanic Systems and Components 5 (1996) 293-298. Ovaj rad se citira i u:

2. Gerlach, G. and Klein, A., "Strategies of modelling and simulation of microsystems with electromechanical energy conversion", Microelectronics Journal**,** Volume 29, Issue 11, November 1998, Pages 773-783.

xxiv) U radu: Wang, F., and Zhang, Q.-j., "*Knowledge-based Neural Models for Microwave Design*", IEEE Trans. on MTT, Vol. 45, No. 12, Dec. 1997, pp. 2333-2343, kaže se: "It has been applied to efficient modelling microwave components, e.g., microstrip interconnections [1]-[3], vias [2], spiral inductors [4], FET devices [5], [6]; ...." gde je pod [5] citiran rad

1. V.B. Litovski, J. Radjenović, Ž.M. Mrčarica, and S. Milenković, "*MOS transistor modelling using neural networks*", Electronic Letters, Vol. 28, No. 18, 1992, pp. 1766-1768. Analizom literature u radovima gospođice F. Wang i njima sličnih, može se lako zaključiti da je rad Prof. Litovskog i saradnika, koji ovde pominjemo, prvi uopšte koji opisuje upotrebu neuronskih mreža u modelovanje elektronskih komponenata i kola.

Do istog se zaključka dolazi i na osnovu:

2. Wang, F. et all., "*Neural network structures and training algorithms for microwave applications*", Int. Journal RF and Microwave CAE, Vol. 9, pp. 216-249, 1999,

3. Wang, B.-Z."*Artificial neural network models for coaxial to waveguide adapters*" International Journal of Infrared and Millimeter Waves, Vol. 20. No. 1. 1999, pp. 125-136.

4. Devabhaktuni, V., et all., "*Neural networks for microwave modelling: model development issues and nonlinear techniques*", Int. Journal RF and Microwave CAE, Vol. 11, pp. 4-21, 2001. (invited review paper).

5. Watson, P.M.; Gupta, K.C., "*EM-ANN models for microstrip vias and interconnects in dataset circuits*", IEEE Transactions on Microwave Theory and Techniques, Volume 44, Issue 12, Dec. 1996 Page(s):2495 – 2503.

6. Jianjun Xu; Yagoub, M.C.E.; Runtao Ding; Qi Jun Zhang, "Exact adjoint sensitivity analysis for neural-based microwave modeling and design", IEEE Transactions on Microwave Theory and Techniques, Volume 51, Issue 1, Jan 2003, pp. 226 – 237. 10.1109/TMTT.2002.806910

7. Hammouda, H.B., Mhiri, M., Gafsi, Z., and Besbes, B., "Neural-Based Models of Semiconductor Devices for SPICE Simulator, American Journal of Applied Sciences Vol. 5, No. 4, pp. 385-391, 2008. ISSN 1546-9239

Do sličnog zaključka dolazi se i u magistarskim tezama:

8. Homayun, F., "*Development of A Library of Neural Models for Microstrip Line Components for High Frequency Circuit Design*", Ottawa-Carleton Institute for Electrical Engineering, Department of Electronics, Carleton University, Ottawa, Ontario KI S SB6, Canada,

http://www.collectionscanada.ca/obj/s4/f2/dsk1/tape8/PQDD_0027/MQ52389.pdf.

9. (magistarska teza) Xi, C., "*Optimization Approaches to the Training of Neural Networks with RFtMicrowave Applications*", Ottawa-Carleton Institute for Electrical and Computer Engineering, Department of Electronics, Carleton University, Ottawa, Ontario Kl S SB6,Canada, 1999

http://www.collectionscanada.ca/obj/s4/f2/dsk1/tape8/PQDD_0018/MQ48465.pdf

10. Wang, F., Devabhaktuni, V.K., Zhang, Q.-J., "*A hierarchical neural network approach to the development of a library of neural models for microwave design*", IEEE Transactions on Microwave Theory and Techniques**,** Volume 46, Issue 12 PART 2, 1998, pp. 2391-2403**.**

11. Tong, Q., Zou, X., and Tong, H., " MOSFET Life Model and NOME Distribution", http://public.whut.edu.cn/slx/English/HongKongConference/MOSFET.pdf

12. Tong, Q., Zou, X., Tong, H., and Liu, T., "Parameter Estimate by Incomplete Neural Network for MOSFET Life Model with NOME Distribution", Proc. of the Third International Conference on Natural Computation (ICNC 2007), Vol. III, 2007, pp. 318-322.

13. Wang, F., Devabhaktuni, V. K., Xi, C, Zhang, Q.-J., "*Neural Network Structures and Training Algorithms for RF and Microwave Applications*", Int. J. RF and Microwave CAE, No. 9, pp. 216-240, 1999, John Wiley & Sons, Inc.

xxv) U radu: Engelbrecht, A.P. and Ismail, A., "*Training Product Unit Neural Networks"*, Stability and Control: Theory and Applications, Vol 2, No 1-2, pp 59-74, 1999, ISSN 1563-3276, kao referenca [16] navodi se da su po prvi put upotrebljene sinapse drugog reda u veštačkim neuronskim mrežama u radu: Milenkovic, S., Obradovic, Z., and Litovski, V., "*Annealing Based Dynamic Learning in Second-Order Neural Networks*", International Conference on Neural Networks, ICNN '96, Washington, D.C., USA, 3.-6. June, 1996, pp. 458-463.

2. Isti rad kao refernca [12] citira se i u: A. Ismail A. and Engelbrecht, A. "*Training Product Units in Feedforward Neural Networks using Particle Swarm Optimization*". In Proceedings of the International Conference on Articial Intelligence, Durban, South Africa, pages 36-40, 1999

i

3. Ismail, A., and Engelbrecht, A.P., "*Global optimization algorithms for training product unit neural networks*", IJCNN, 2000.

xxvi) U radu Pietrenko, W., Janke, W., and Kazimierczuk, M., "*Application of Semianalytical Recursive Convolution Algorithms for Large-Signal Time-Domain Simulation of Switched-Mode Power Converters*", IEEE Trans. on Circuits and Systems - I: Fundamental Theory and Applications, Vol. 48, No. 10, October 2001, pp. 1246-1252, kaže se "The difficulties of handling the Dirac delta impulses and the methods to overcome them are discussed in [2]-[5]. Referenca [5] je: Mrčarica, Ž., Ilić, T., and Litovski, V., "*Time-Domain Analysis of Switched networks with internally controlled switches*", IEEE Trans. on Circuits and Systems - I: Fundamental Theory and Applications, Vol. 46, No. 3, March 1999, pp. 373-378.

Isti rad se citira i u

2. Demir, Y, and Koksal, M., "*State space suitable modelling of power semiconductors with ideal switches, resistors, constant voltage and current sources*", Electronic Engineering (Archiv fur Elektrotechnik), Vol. 86, No. 3, Feb. 2004, pp. 135-145, kao i u
3. Herdem, S., and Köksal, M., "*A fast algorithm to compute the steady-state solution of nonlinear circuits by piecewise linearization*",Computers & Electrical Engineering, Volume 28, Issue 2, March 2002, Pages 91-101,
4. Cheong, S.V. Chung, S.H. Ioinovici, A. **"***Duty-cycle control boosts DC-DC converters*" Circuits and Devices Magazine, IEEE**,** Mar 1993, Volume: 9, Issue: 2, On page(s): 36-37, ISSN: 8755-3996.
5. Francisco del Águila López, Pere Palà Schönwälder, Jordi Bonet Dalmau y Rosa Giralt Mas, "*Técnica de Análisis de Circuitos Conmutados no Lineales con Topologías Independientes*",

http://w3.iec.csic.es/ursi/articulos_coruna_2003/actas_pdf/SESION%202/S2.%20Aula%202.2/1499%20-%20TECNICA%20DE%20ANALISIS.pdf kaže se: Para superar estas dificultades existen algunas técnicas que utilizan modelos específicos de conmutadores [3], gde je referenca [3]: Mrčarica, Ž., Ilić, T., Litovski, V., "*Time-Domain Analysis Of Nolinear Switched Networks With Internally Controlled Switches*", IEEE Transactions on Circuits and Systems I, Vol. 46, No. 3, March, 1999, pp. 373-378.

Slično se tvrdi i u:

6. F. Del Aguila Lopez, P. Pal Schonwalder, and J. Bonet Dalmau, Mas, R.G, "*A discrete-time technique for the steady state analysis of nonlinear switched circuits with inconsistent initial conditions*", The 2001 IEEE International Symposium on Circuits and Systems, 2001. ISCAS 2001, Volume 3, Issue , 6-9 May 2001, pp. 357 - 360 vol. 2. i u
7. del-Aguila-Lopez, F.; Pala-Schonwalder, P.; Molina-Gaudo, P.; Mediano-Heredia, A.; "*A Discrete-Time Technique for the Steady-State Analysis of Nonlinear Class-E Amplifiers*"**,** IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, Volume 54, Issue 6, June 2007 Page(s):1358 - 1366

kao i u

8. Herdem, S. and Köksal, K., "*Fast algorithm to compute the steady-state solution of nonlinear circuits by piecewise linearization*", Computers & Electrical Engineering , Elsevier, Volume 28, Issue 2 , March 2002, pp. 91-101.
9. Luhuai MA Xi Zhao Wei Yin, "*Piecewise linear analysis of network switching nodes Equations*", Journal of XI 'AN Jiaotong University, 2002, Vol.36, No.6, pp.559 – 563.
10. Acciani, G., Chiarantoni, E., Fornarelli, G., and Vergura, S., "*An Homotopy Function for Transient Analysis of Switching Circuits*", IEEE ISIE 2005, June 20-23, 2005, Dubrovnik, Croatia, pp. 595-600. 0-7803-8738-4/05/$20.00 ©2005 IEEE.
11. Welsch, G. Brachtendorf, P.G. Sabelhaus, C. Laur, R. "*Minimization of the error in the calculation of the steady state byshooting methods*", IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, Oct. 2001, Vol. 48, No. 10, pp. 1252-1257, ISSN: 1057-7122.
12. Pietrenko, W., Janke, W., Kazimierczuk, M.K., "*Application of semianalytical recursive convolution algorithms forlarge-signal time-domain simulation of switch-mode power converters*", IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, Volume 48, Issue 10, October 2001, Pages 1246-1252.
13. Wang, S, et all., "*An improved V-A characteristics of switches and its application in coupled field-circuit simulation of permanent magnet brushless DC motor*", The 4th International Power Electronics and Motion Control Conference, 2004. IPEMC 2004.14-16 Aug. 2004, Volume: 2, pp. 1013- 1017, ISBN: 7-5605-1869-9.
14. del Aguila, F.; Pala, P.; Bonet, J.; Xavier Moncunill, F.; Giralt, R., "*Analysis of Nonlinear Switched Circuits with Different State Variables in Each Topology*", 14th IEEE International Conference on Electronics, Circuits and Systems, 2007. ICECS 2007, 11-14 Dec. 2007, pp:1039 – 1042
15. Yin, Youwei; Zhao, Luhuai; Ma, Xikui**, "***Novel Method for the Analysis of Piece-Wise Linear Switched Networks Based on Differential Nodal Equations*", Journal of XI'AN Jiaotong University 2002, Vol.36 No.6 pp. 559-563.
16. Liao, W., Tian, F., and Liu, J., "Efficient fault diagnosis method in nonlinear circuits based on neural network", Computer Engineering and Applications, Vol 45, No.19, 2009, pp. 228-231.

xxvii) U izveštaju: "Kharti, S.P., Mehrotra, A., Prasad, M.R., Brayton, R.K., and Sangiovani-Vincentelli, A., *Routing Techniques for Deep Sub-micron Technologies*", Laboratorije za projektovanje elektronskih kola **Univerziteta u Berkeley**-u, Kalifornia, USA, (*http://www-cad.eecs.berkeley.edu/čmukul/reports/mr.ps*), koji je objavljen 16.03.1999. god, kaže se: "Area routing techniques have been reviewed as part of several surveys on physical design [KO90, Oht86, DL89]". Sa [DL89] je citiran rad: Damnjanović, M.S., and Litovski, V.B., "*A survey of routing algorithms in custom IC design*", Journal of Semicustom ICs, Vol. 7, No. 2, 1989.

xxviii) U pregledu softvera za projektovanje u tekstilnoj industriji, na vietnamskoj web stranici: (*www.cesti.gov.vn/webcms/jsp/ download/maydetjacquard.htm*), pominju se pet paketa od kojih jedan (JUD-GE) je razvijen u LEDA pod rukovodstvom Prof. Litovski, a opisan u radu: Zarković, K., Ranđelović, Z., Milenković, S., Novaković, M., Jovanović, Lj., Litovski, V., *"JUDGE - Jacquard Developing Environment (Editor)"*, Tekstilna industrija, 3-4/97, Beograd, 1997.

xix) U radu: Endemano, A., Fourniols J. Y., Camon H., Marchese A., Muratet S., Bony F., Dunnigan M., Desmulliez M. P. Y., and Overton G. **(Mentor Graphics (UK) Ltd,** Rivergate, Newbury Business Park, London Road, Newbury, Berkshire RG14 2QB, UK) "*VHDL-AMS modelling and simulation of a planar electrostatic micromotor*", J. of Micromechanics and Microengineering, Vol. 13, 2003, pp. 580-590, kaže se "Their use, however, requires a substantial understanding of the underlying physical behavior and ...[4-6]. Pod [5] se citira: Damnjanović, M., Dimić, Ž., Litovski, V., and Glozić, D., "*Hardware description language for Alecsis simulator*", Proc. of the 20th Conf. on Microelectronics, 1995, Vol. 2., pp. 525-528.

xxx) U radu Zhang, T. **(Cadence Design Systems, Inc., Cary, NC 27511 USA.**), Chakrabarty, K., and Fair, R.B., "Behavioral modeling and performance evaluation of microelectrofluidics-based PCR systems using SystemC", IEEE Trans. on CAD of Integrated circuits and Systems, Vol. 23, No. 6, June 2004, pp. 843-858, kaže se: “We adopt the strategy of trading-off behavioral fidelity with the efficiency of analysis, "blinding" unnecessary low-level detail, and paying more attention to certain tractable subsystems [42]. “ Pod [42] se citira: Ž. Mrčarica, V. B. Litovski, M. Jakovljević, H. Detter, "*Hierarchical modelling of microsystems in an object-oriented HDL*", Proc. of the 21st Int. Conf. On Microelectronics, MIEL'97, Niš, Yugoslavia, September 1997, pp. 475-478.

Isti rad se citira i u knjizi:

2. Zhang, T., Chakrabarty, K. and Fair, R. B., “A Hierarchical Design Platform for Microelectrofluidic Systems (MEFS), Springer US, 2006, ISBN 978-0-387-24520-1 (Print) 978-0-387-25786-0 (Online), kao i rad:

xxxi) U radu: L. Capodieci, R. Subramanian, B. Rangarajan , W. D. Heavlin, J. Li, D. A. Bernard, and V. V. Boksha, " *Novel methodology for postexposure bake calibration and optimization based on electrical linewidth measurement and process metamodeling*", Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures, November 1998 , Vol. 16, No. 6, pp. 3752-3758, citira se: Pantić, D., Milenković, S., Trajković, T., Litovski, V., Stojadinović, N., *"Inverse Modeling Of Semiconductor Manufacturing Processes"*, 20th Int. Conference on Microelectronics MIEL '95, Vol. 1, Niš, 12-14 Sep., 1995, pp. 321-326.

Isti rad se citira i

2. u magistarskoj tezi: Chiang, M.-L., "*Process Recipe Optimization in Multiple Response System*", Chung Yuan Christian University, Department of Mechanical engineering, 2001 (URN: etd-0813102-120054), kao i u

3. Flax, M.R. Jin, J.S. **"**A matrix approach to neural network inversion", Proceedings of the ICONIP '99. 6th International Conference on Neural Information Processing, Publication Date: 1999, Volume: 1, On page(s): 85-90 vol.1, Meeting Date: 11/16/1999 - 11/20/1999, Location: Perth, WA, Australia.

xxxii) U radovima Hofmann, K., Glesner, M., Sebe, N., Manolescu, A., Marco, M., Samitier, J., Karam, J.-M., Courtois, B., "*Generation of the HDL-A-model of a Micromembrane from its Finite-element-description*", ED&TC'97, Paris, France, pp.108--112, March, 1997 , i

2. Karam, J.M., Courtois, B., Boutamine, H., Drake, P., Rencz, M., Poppe, A., Szkely, V., Hofmann, K., Glesner, M., "*CAD and foundries for microsystems*", Proceedings of the 1997 Design Automation Conference, Anaheim, CA, June 1997, pp. 674-679,

citira se kao prva referenca: Mrčarica, Ž., Detter, H., Glozić, D., Litovski, V., *"Describing Space-Continous Models Of Microelectromechanical Devices For Behavioural Simulation"*, European Design Automation Conference, EURO-DAC '96 with EURO-VHDL '96, Geneva, 16-20 Sep., 1996, pp. 316-321.

3. Isti rad se citira i u Hans-Joachim Bungartz, Anton Frank, Florian Meier, et al., "*Fluid Structure Interaction: 3D Numerical Simulation and Visualization of a Micropump*", TUM-19710, as a chapter in "*Methoden und Werkzeuge fuer die nutzukg paralleler Architekturen*", published by: Fakultaet fuer Informatik der TechnischenUniversitaet Muenchen, 1997

4. i u: Bungartz, H.-J., Frank.A, and Meier, F., "Design and Implementation of a Modular Environment for Coupled Systems", u okviru: "Matematische modelirung , simulation und verification in materialorientierten Prozessen und intelligenten systemen", Sonderforschungsbereich 438, Technische Universitaet Muenchen, Universitaet Augsburg, April 1998.

5. kao i u: Ramaswamy, D., "Simulation Tools for MicroElectroMechanical System", Ph.D. Thesis, MIT, Boston, MA, May 2001

xxxiii) U radu: Melekian, V., " Logic Simulation of Digital Circuits Exposed to Radiation", Facta Universitatis, Series: Electronics and Energetics, Vol. 12, No.1 (1999), 71-86, UDC 621.3.049.7, citiraju se sledeći naslovi:

1. P. Petkovic, et al.: "*VLSI Design*", Nauka, Beograd, 1991. (in Serbian)
2. V. Litovski and M. Zwolinski,: "*VLSI Circuit Simulation and Optimization*", Chapman and Hall, 1997.
3. Litovski, et al.: "*Analysis of bipolar and MOS circuits using program MOST*", Proc. of 16th Yugoslav Conference on Microelectronics, MIEL 88, Zagreb, 1988, pp. 303-310. (in Serbian)

xxxiv) George Mason University, Fairfax, Virginia, Dept. Electrical and Computer Engineering, u projektnom zadatku ECE 645 "*Area optimized square root and dividet unit for multimedia processing application*", autora Reddy, S. and Srivastava, U., citira se:

1. B. Jovanović, M. Damnjanović, V. Litovski, „Square Root on Chip", ETF Journal of Electrical Engineering, A Publication of the EE Department, University of Montenegro May 2004 Vol.12 No.1 YU ISSN: 0353-5207

http://ece.gmu.edu/courses/ECE645/projects_S05/specs/SQR_DIV_shilpa_utkarsh.pdf

isti rad se citira i u

2. Naji, H.R., "Solving Complex Computational Problems Using Multiagents Implemented in Hardware," *Computing in Science and Engineering*, Vol. 10, No. 5, pp. 54-63, Sep./Oct. 2008, doi:10.1109/MCSE.2008.121.

xxxv) Rad: Litovski, V., Mrčarica, Ž., Ilić, T., *"Simulation Of Non-Linear Magnetic Circuits Modelled Using Artificial Neural Network"*, Journal Simulation Practice and Theory, Vol. 5, No. 6, 1997, pp. 553-570, citira se u

1. "Magnetic Resource Directory", *http://www.magnetsmagnetic.info/magneticcircuits/*
2. Sutanto, J., Setia, R., Papania, A., May, G.S., Hesketh, P.J., and Berthelot, Y.H., "*Using neural networks to model an electromagnetic-actuated microactuator*", J. Micro/Nanolith. MEMS MOEMS 6, 013011 (2007)
3. Nouir, Z., Sayrac, B., Fourestie, B., Tabbara, W., and Brouaye, F., "*Generalization Capabilities Enhancement of a Learning System by Fuzzy Space Clustering* ", Journal of Communications, Vol. 2, No. 6, Nov. 2007, pp. 30-37.

xxxvi) University of Rostock, Germany, Department of Microelectronics & CE, u okviru: *Project: ntegrated Circuit Design 1, Task:* Power Operation Amplifier, *Technology:* CMOS-Technology, *Mentor: Prof. Dr. Beikirch, Student:* Dejan Vidanovic, Matri. No. – 4299525, citira: V. Litovski, *Elektronika I.*

http://users.verat.net/~simeone/Project%20Integrated%20Circuit%20Design%201.pdf

xxxvii) U magistarskoj tezi: Karlsson, M., "*Test system for improved hardware tests*", (A master of science thesis project done in cooperation with Mälardalens University and ABB robotics), http://www.idt.mdh.se/utbildning/exjobb/files/TR0552.pdf citira se:

1. Panić, V., Janković, S., Milovanović, D., Litovski, V., "*Cell Design for Boundary-Scan Implementation* ", 22nd Int. Conf. on Microelectronics, MIEL '99, Niš, Yugoslavia, May, 2000, pp. 719-722.
2.

xxxviii) U radu: Parsons, David (2006) 'The Environmental Impact of Electronics and Its Incorporation into the Curriculum.' in: 17th Annual Conference of the Australasian Association for Engineering Education, 10-13 December 2006, Auckland, New Zealand, citira se:

1. Milojković, J.B. and Litovski V.B."*Eco Design in Electronics – The State of the Art*." Working and Living Environmental Protection Vol. 2, No 2, 2002, pp. 87 – 100.

Isti rad se citira i u

2. Munitlak, Đ., "*Model upravljačkog sistema u zaštiti životne sredine i održivog korišćenja resursa*», Doktorska disertacija, Asocijacija centara za interdisciplinarne i multidisciplinarne studije i sitraživanja, Centar za inžinjerstvo za zaštitu životne sredine, Novi Sad, 2007.
3. Amitava Bandyopadhyay, "A regulatory approach for e-waste management: a cross-national review of current practice and policy with an assessment and policy recommendation for the Indian perspective**"**, International Journal of Environment and Waste Management, Volume 2, Number 1-2 / 2008, pp. 139 – 186,
4. Nnorom, I.C., et all., "Achieving Resource Conservation in Electronic Waste Management: A Review of options Available to Developing Countries", Journal of Applied Sciences, ISBN 1812-5654, Vol. 20, No. 7, 2007, pp. 2918-2933.
5. Chongwatpol, J., "Analysis of waste electrical and electronic equipment (WEEE) in Thailand and implementation of risk management plan to comply with future WEEE regulations", Magistaska teza, The Graduate School, University of South Visconsin, USA, 2004.
6. da Fonseca, C.G.P., "Ecodesign e a reutilização de computadores", Magistarska teza, Faculdade de Engenharia da Universidade do Porto, Portugal, 2007.

xxxviii) U radu: Asgary, R., Mohammadi, K. and Zwolinski, M., "Using neural networks as a fault detection mechanism in MEMS devices". *Microelectronic Reliability* Vol. 47, No. 1, pp. 142-149,

citira se

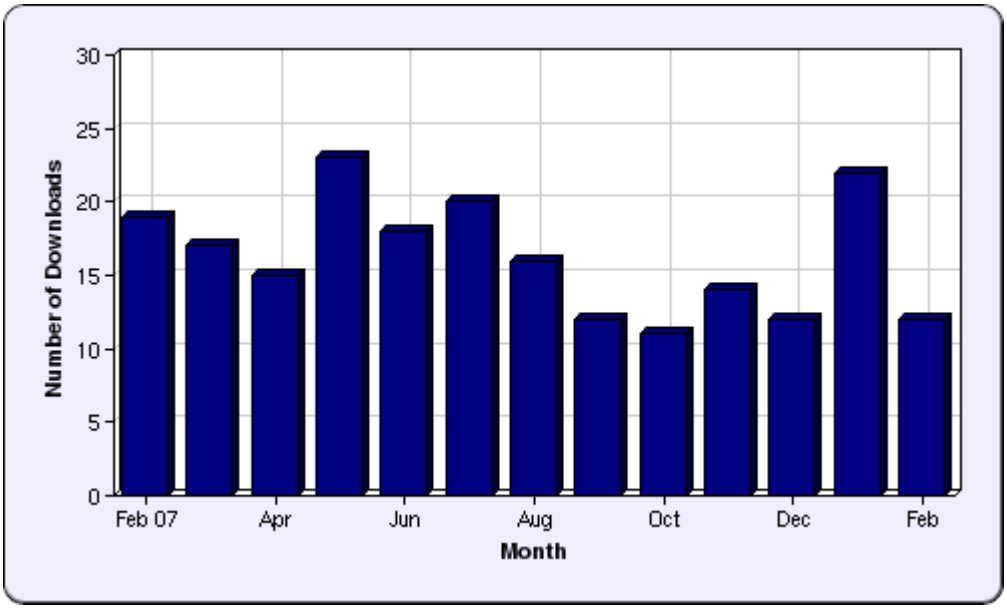
1. Litovski V, Andrejevic M, Zwolinski M. "Behavioural modelling, simulation, test and diagnosis of MEMS using ANNs", In: Proc Intl Symp Circuits and Systems, Kobe, Japan, 2005, pp. 5182-5185.

Isti rad se citira i u doktorskoj disertaciji

2. Basheer, N. Z. A., "*An investigation of delay fault testing for multi voltage design*", University of Southampton, Faculty of Engineering, Science and Mathematics, School of Electronics and Computer Science, 2009,

3. kao i u studiji: Deesiri **, A., "***Testing and improving Micro accelerometer for Micro Electromechanical Systems (MEMS) design*", Department of Electrical Engineering, Faculty of Engineering, Sripatum University, Year of Publication : B.E. 2008.

Na slici je histogram download-ovanja ovog rada sa baze radova Univerziteta u Southamptonu za 2007/2008. god. Naslov slike je: *Dashboard for Litovski, V., Andrejević, M. and Zwolinski, M. (2005)* Behavioural Modelling, Simulation, Test and Diagnosis of MEMS using ANNs. *In: International Symposium on Circuits and Systems, 23-26 May 2005, Kobe, Japan.*



xxxix) U radu: Damiano, J.-P. Scotto, M. Ribero, J.-M., "Computer-algebra systems and electromagnetic problems", IEEE Antennas and Propagation Magazine, Publication Date: Dec 1996, Volume: 38, Issue: 6, On page(s): 92-98, ISSN: 1045-9243, citira se: Marković, V., Petković, P., Litovski, V., *"Symbolic Approach To The Microwave Circuit Design"*, XI International Microwave Conference MICON '96, Warsaw, 27-30 May, 1996. Isti rad se citira i u

2. Damiano, J.-P. and Ghio, G. , "*Computer algebra systems applied to some electromagnetic problems*", Annales des Telecommunications/Annals of Telecommunications , Volume 52, Issue 5-6, May 1997, Pages 306-318.

xL) U radu: Minjie, M., Zheying, L., Guangyu, J., "*Study on analyzing and modeling of delay activity for digital circuit*", ASICON 2005: 2005 6th International Conference on ASIC, Proceedings**,** Volume 2, 2005, Article number 1611420, Pages 681-684**,**

citira se

1. Maksimovic, D.M., Litovski, V.B., "*Timing Simulation with VHDL Simulators*" (2002) Proc.23rd International Conference on Microelectronics (MIEL 2002), (NIS, 2. YUGOSLAVIA. 12-15 May,

2. Maksimović, D.M., Litovski, V.B., "*Logic simulation methods for longest path delay estimation*", (2002) *IEE Proceedings: Computers and Digital Techniques*, 149 (2), pp. 53-59

poslednji se rad citira i u:

3. Li, Z., Ma, M., Li, Z., "*Study on detecting of competition phenomena of signal for logic combinational circuit*", International Conference on Signal Processing Proceedings, ICSP, Volume 4, 2007, Article number 4129831

xLi) U radu: Sutanto, J., Setia, R., Papania, A., May, G. S., Hesketh, P.J., and Berthelot, Y. H., "Using neural networks to model an electromagnetic-actuated microactuator" Journal of Micro/Nanolithography, MEMS and MOEMS , January - March 2007, Volume 6, Issue 1, pp. 13011-13021, citira se: V. Litovski, M. Andrejevic, M. Zwolinski, "ANN Based Modeling, Testing, and Diagnosis of MEMS," *IEEE 7th Seminar on Neural Network Applications in Electrical Engineering*, 183-188, Sept (2004)

xLii) Knjiga: V.B. Litovski: CAD of electronic circuits, DIGP "Nova Jugoslavija", Vranje, 2000 (in Serbian) citirana je u

1. Topisirović, D., "Advances in VLSI Testing at MultiGb per Second Rates", Serbian Journal Of Electrical Engineering, Vol. 2, No. 1, May 2005, 43 – 55.

xLiii) U radu: Osibanjo O., and Nnorom, I.C. **«***The challenge of electronic waste (e-waste) management in developing countries*", Waste Management & Research, Vol. 25, No. 6, 489-501 (2007), DOI: 10.1177/0734242X07082028, © 2007 International Solid Waste Association, citira se:

1. Milojković, J., and Litovski, V., "*Concepts of computer take-back for sustainable end-of-life*", Facta Universitatis, Series: Working and Living Environmental Protection, Vol. 2, No. 5, 2005, pp. 363-372. isti rad se citira i u :
2. Nnorom I.C., and Osibanjo, O. "*Overview of electronic waste (e-waste) management practices and legislations, and their poor applications in the developing countries*", Resources, Conservation and Recycling, Vol. 52, No. 6, April 2008, pp. 843-858, kao i u
3. Osibanjo, O. and Nnorom, C. I., "*Material flows of mobile phones and accessories in Nigeria: Environmental implications and sound end-of-life management options*", Environmental Impact Assessment Review, Vol. 28, No. 2-3, February-April 2008, pp. 198-213,
4. Wagner, T. P., "*Shared responsibility for managing electronic waste: A case study of Maine, USA***",** Waste Management, Vol. 29, No. 12, Dec. 2009, pp. 3014-3021
5.

xLiv) U US patentu: MIXED SIGNAL SIMULATION - Patent EP1305765, citira se: Litovski, V., Dimić, Ž., Damnjanović, M., Mrčarica, *Ž., "Electronic Circuit Simulation In A Mixed-Language Environment*", Miroelectronics Journal, Vol. 29, No. 8, 1998, pp. 553-558

xLv) U radu: Yao, Kai-chao Liao, Chin-wen Chao, Li-ling Lin, Fu-yu, "*Virtual Impedance Analyzer Design and Implementation*", Second International Conference on Innovative Computing, Information and Control, 2007. ICICIC '07. Publication Date: 5-7 Sept. 2007, On page(s): 71-71, Location: Kumamoto, Japan, ISBN: 0-7695-2882-1, citiraju se radovi :

1. Dimitrijevic, M., Litovski, V., Jovanovic, S., "*Computer system for laboratory exercises in electronics*"**,** (2004) *Proc. of 5th Conference of Indel*, pp. 156-160.in Serbian, i

2. Dimitrijevic, M., Litovski, V.”*Computer integrated analogue electronics laboratory for undergraduate teaching”, Proc. of REV 2005 Conference* Brashov, Romania, proc. on CD.

xLvi) U radu: . Mohammadi, K., and Seyyed Mahdavi, S.J., “*On improving training time of neural networks in mixed signal circuit fault diagnosis applications*”, Microelectronics and Reliability, 2008

citira se

1. Litovski VB, and Andrejevic M., “*Electronic modelling using ANNs for analogue and mixed-mode behavioural simulation*”, Invited paper, In: 6th Seminar on neural network applications in electrical engineering, NEUREL ’02; 26–28 September 2002. p. 113–8.
2.

xLvii) U patentu: Jones, K.D. (Hayward, CA, US), Sheffler, T. J. (San Francisco, CA, US), Mossawir, K. M. (Stanford, CA, US), Hong, Q. (San Jose, CA, US), Wong, P.(San Jose, CA, US), Jiang, J. (Stanford, CA, US), **«** *Mixed mode verifier* **»,** Number: United States Patent 7360187 , citira se Litovski, V. B., Andrejević, M., Petković, P., Damper, R., “*ANN Application to Modelling of the D/A and A/D Interface for Mixed-Mode Behavioural Simulation*”, Journal of Circuits, Systems and Computers, Vol. 13, No. 1, February 2004, pp. 181-192.

xLviii) U radu: Batard, C. , Poitiers, F. and Machmoum, M., « *An Original Method to Simulate Diodes Rectifiers Behaviour with Matlab-Simulink Taking into Account Overlap Phenomenon*”, IEEE International Symposium on Industrial Electronics, 2007. ISIE 2007. 4-7 June 2007, pp. 971-976, Vigo, Spain,ISBN: 978-1-4244-0755-2 citira se

1. V. Litovski, M. Savic, Z. Mrcarica ‘*Electronic circuit simulation with ideal switches*’, July 2005, *HAIT Journal of Science and Engineering B*, pp. 476-495.
2. Isti rad se citira i u: Sheffler, T.J. “*Design of a Switch-Level Analog Model for Verilog*”, IEEE Int. Behavioral Modeling and Simulation Workshop, BMAS 2008, September 2008, pp. 118-123, DOI 10.1109/BMAS.2008.4751252
3.

iL) Rad: Andrejević, M., Litovski, V., "*ANN Aplication In Modelling of Chua's Circuit*", Proc. of Neurel 2002, Belgrade, September 2002, pp. 119-122 citira se u:

1. Dalkiran, I. Dalkiran, F.Y. Danisman, K. Kilic, R., Erciyes Univ. Muh., Kayseri;, “*Prediction of Dynamics of Chaotic Chua's Circuit with Artificial Neural Network*”, SIU 2007. IEEE 15th Signal Processing and Communications Applications, 2007., June 2007, pp. 1-4, Location: Eskisehir.

L) Rad: V. B. Litovski, I. V Litovski and M. Zwolinski, “*Concurrent analogue fault simulation, the equation formulation aspect*”, International Journal of Circuit Theory and Applications, 32(6), 487-507 (2004). citira se

1. U prijavi projekta: “Meeting the Design Challenges of Nano-CMOS Electronics”, pri EPSRC (Electronics and physics research council), od strane: Institute for Integrated Micro and Nano Systems (IMNS), School of Engineering and Electronics, Science and engineering at the University of Edinbrough.
   www.see.ed.ac.uk/~afm/tmp/eScience.pdf, kao i u radu
2. Garczarczyk, Z.A. , “Polynomial fault diagnosis of linear analog circuits”, 18th European Conference on Circuit Theory and Design, 2007. ECCTD 2007, Seville, 27-30 Aug. 2007, pp. 842-845, ISBN: 978-1-4244-1341-6, DOI: 10.1109/ ECCTD.2007.4529728.

Li) Rad: Anđelković, B., Litovski, **V.,** and Zerbe, V., “*Mission Level Modeling And Simulation Language For Mixed-Signal System-On-A-Chip Design*", Journal of Circuits, Systems and Computers (World Scientific Publishing Company), Vol. 16, No. 1, February 2007, pp. 15-28.

1. citira se u okviru web stranice:

http://www.mirrorservice.org/sites/home.ubalt.edu/ntsbarsh/Business-stat/RefSim.htm, čiji je naslov: Modeling & Simulation Resources. Podnaslov u kome se rad citira je: Journal Articles.
2.

Lii) RAD: Stefanovic D., Kayal M., Pastre M., Litovski V. B. "*Procedural Analog Design (PAD) Tool*", Proc. ISQED'03. 2003.

citira se u

1. Зинченко, Л.А., "Интеллектуальные системы схемотехнического проектирования**",** Десятая национальная конференция по искусственному интеллекту с международным участием, КИИ-2006, Обнинск, 25-28 сентября 2006 года, www.raai.org/resurs/papers/kii-2006/seminar/Zinchenko.doc, УДК 621.372.
2. www.grabinski.ch/GMC (wladek@grabinski.ch), "EKV Modeling Engineering Support", http://legwww.epfl.ch/ekv/workshop/papers/03_W_Grabinski_1st_WS_NE.pdf.

Liii) Rad: Jakovljević, M., Mrčarica, Ž., Fotiu, P., Detter, H., **Litovski, V.**, "*Transient Electro-Thermal Simulation Of Microsystems With Space-Continuous Thermal Models In Analogue Behavioural Simulator*", Microelectronics and Reliability, Vol. 40, No. 3, March 2000, pp. 507-516, citira se u

1. Liu, G., Wang, A., Jiang, T., Jiao, J., Jang, J.B., „*Effects of environmental temperature on the performance of a micromachined gyroscope*", Microsystem Technologies (Springer), Volume 14, Number 2 / February, 2008, pp. 199-204.
2.

Liv) Rad: Petković, P., Milovanović, D., **Litovski, V.**, *"Symbolic Fault Modelling And Test Generation Of MOS Circuits"*, Microelectronics and Reliability, Vol. 37, No. 1, 1997, pp. 137-157.

Citira se u:

1. Žemva, A., and Zajc, B., "Test generation for technology-specific multi-faults based on detectable perturbations", Microelectronics Reliability, Vol. 45, No. 1, Jan. 2005, pp. 163-173,
2.

Lv) U radu: Pang, K.K. and Kirton, P.A., "*Optimum flat delay filter characteristics***",** International Journal of Circuit Theory and Applications, Volume 10 Issue 4, Pages 361 – 375, citira se:

1. Litovski, V.**,** *"Synthesis Of Monotonic Passband Sharp Cutoff Filters With Constant Group Delay Response"*, IEEE Trans. on Circuits and Systems, Vol. CAS-26, No. 8, 1979, pp. 597-602.

Lvi) u radu: Petlenkov, E., Jutman, A., Nomm, S., and Ubar, R. „*Towards artificial intelligence based automatic adaptive response analyzer for high frequency analog BIST*", Proc. of 2008 IEEE International Conference on Computational Intelligence for Measurement Systems and Applications, 2008. CIMSA 2008. 14-16 July 2008, pp. 99-104, Istanbul, ISBN: 978-1-4244-2305-7, Citira se:

1. Litovski, V.**,** Andrejević, M., and Zwolinski, M. "*Analog electronic circuit diagnosis based on ANNs* ", Microelectronics Reliability, Vol. 46 (2006), pp. 1382-1391.

isti rad se citira i u

2. Jantos, P., Grzechca, D., Rutkowski, J., *"Global Parametric Fault Identification In Analog Electronic Circuits*", Metrology And Measurement Systems, Vol. XVI, No. 3, 2009, *Paper No. M 0310.* ISSN 0860-8229, *www.metrology.pg.gda.pl*,,
3. Kuczynski, A., and Ossowski, M., "*Circuit Fault Diagnosis Based on Wavelet Packet and Neural Network*", Proceedings of ISTET 2009, VXV International Symposium on Theoretical Engineering, Lübeck, Germany, June 2009, pp. 114-117.

Lvii) U radu: Yao, Kai-chao, **"**PC-Based virtual bode analyzer design and application in automatic measurement of filter manufacturing**",** ICIC Express Letters, Volume 3, Number 1, March 2009, pp. 33—40, ISSN 1881-803X**,** citiraju se radovi :

1. Dimitrijevic, M., Litovski, V., Jovanovic, S., *"Computer system for laboratory exercises in electronics*"**,** (2004) *Proc. of 5th Conference of Indel*, pp. 156-160.in Serbian, i
2. Dimitrijevic, M., Litovski, V."*Computer integrated analogue electronics laboratory for undergraduate teaching"*, *Proc. of REV 2005 Conference* Brashov, Romania, proc. on CD.

Rad pod brojem **Lvii**.1. citira se i u

3. Јовица Милисављевић, мр. Александар Поповић ,"*Сет наставних комплета "Физика помоћу рачунара""*, Републички семинар о настави физике 2006, Beograd, pp. 1-4.

Lviii) U radu: Nagy, G., Horváth, G. and Poppe, P., "Consideration of Thermal Effects in Logic Simulation", Proc of the THERMINIC 2008, 24-26 September 2008, Rome, Italy, pp. 229-234, EDA Publishing, ISBN: 978-2-35500-008-9 229, Citira se:

1. M. Jakovljevic, P. A. Fotiu, Z. Mrcarica, V. Litovski, H. Detter, "*Electro-thermal Simulation of Microsystems with mixed abstraction modeling*",Microelectronics Reliability 41, pp. 823-835, 2001.

Lix) U radu: Зинченко, Л.А., и Сорокин, Б.С., "Бионические информационные системы в проектировании микро- и наносистем", Одинадцатая Национальная Конференция по Искусственному Интеллекту с Международным Участием, г. Дубна, 29 сентября – 3 октября, 2008 года. (Материалы наиболее интересных докладов будут опубликованы в журналах "Искусственный интеллект и принятие решений", "Программные продукты и системы", "Научно-техническая информация" (серия 2).) citira se:

1. Litovski, **V.,** Andrejević, M., and Zwolinski, M., "*ANN based modeling, testing, and diagnosis of MEMS*", Proc. of the 7th Seminar on Neural network Applications in Electronic engineering, NEUREL 2004, Sept. 2004, Belgrade, pp. 183-188. Ovaj rad se citira i u
2. Doktorskoj disertaciji: Deesiri, A., "*Testing and improving Micro accelerometer for Micro Electromechanical Systems (MEMS) design*", Department of Electrical Engineering, Faculty of Engineering, Sripatum University, Bakgkok, Thailand, 2008.
3.

Lx) U patentu: Meyer, S. J., "Mixed signal simulation", Application Number: EP20010954620, Publication Date: 05/02/2003. Citira se :

1. Litovski V., Dimić, Ž., Damnjanović, M., Mrčarica, Ž., " *Electronic circuit simulation in a mixed-language environment*", Microelectronics journal, Mackintosh publications

LTD. Luton, GB, Vol. 29, No. 8, 1 August 1998, pp. 553-558, XP004124661 ISSN: 0026-2692 i

2. Damnjanović, M., Dimić, Ž., Litovski, V., and Glozić, D., "*Hardware description language for Alecsis simulator*", Proc. of the 20th Conf. on Microelectronics, 1995, Vol. 2., pp. 525-528.

Lx) U radu: M[a]de las Mercedes Gómez-Albarrán, Ana M[a] Fernández-Pampillón-Cesteros and Juan Manuel Sánchez-Pérez , "*A routing strategy based on genetic algorithms*", Microelectronics Journal, Vol. 28, No. 6-7, August-September 1997, pp. 641-656, citira se

1. **Litovski, V.**, Ranđelović, Z., Damnjanović, M., *"A Routing In Standard Cells"*, 20th International Conference on Microelectronics MIEL '95, Vol. 2, Niš, 12-14 Sep., 1995, pp. 461-466.

Lxi) U radu: Sindia, S., Singh, V., and Agrawal, V.,"*Bounds on Defect Level and Fault Coverage in Linear Analog Circuit Testing*", 13th IEEE/ VSI VDAT2009 VLSI Design And Test Symposium, July 8-10, 2009, Electonic City, Hosur Road, Bangalore, India, citira se

1. Panić, V., Milovanović, D., Petković, P., **Litovski, V.**, *"Fault Location In Passive Analog RC Circuits By Measuring Impulse Response"*, 20th International Conf. on Microelectronics MIEL '95, Vol. 2, Niš, 12-14 Sep., 1995, pp. 517-520.
2. Isti rad se citira i u radu: Sindia, S., Singh, V., and Agrawal, V.,"*Polynomial Coefficient Based DC Testing of Non-Linear Analog Circuits***",** Proceedings of the 19th ACM Great Lakes symposium on VLSI**,** *GLSVLSI'09*, May 10–12, 2009, Boston, Massachusetts, USA, Pages 69-74 , SBN:978-1-60558-522-2. kao i u
3. Sindia, S., Singh, V., and Agrawal, V., "*Multi-Tone Testing of Linear and Nonlinear Analog Circuits using Polynomial Coefficients*", IEEE Asian Test Symposium (**ATS**) 2009, Taichung, Taiwan, Nov 2009. ATS'09, accepted
4. Sindia, S., Singh, V., and Agrawal, V., "*V-Transform: An Enhanced Polynomial Coefficient Based DC Test for Non- Linear Analog Circuits*", 7th IEEE East-West Design & Test Symposium, EWDTS 2009, Moscow, Russia, September 18 -21, 2009, http://www.eng.auburn.edu/~vagrawal/TALKS/EWDTS09/ewdts09-31.pdf,
5. Sindia, S., Singh, V., and Agrawal, V.," Parametric Fault Diagnosis of Nonlinear Analog Circuits using Polynomial Coefficients", www.eng.auburn.edu/~vagrawal/TALKS/VD10/PID1061303.pdf .
6. Sindia, S., Singh, V., and Agrawal, V., "Polynomial Coefficient Based Multi-Tone Testing of Analog Circuits", Proc. of the 18th North Atlantic *Test Workshop*, pp. 6–15, May 2009. http://www.eng.auburn.edu/~vagrawal/TALKS/ATS09/nft_ieee.pdf

Lxii) U radu: Grasso, F., Manetti, S., and Maria Cristina, P.M., "*A symbolic approach to design centering of analog circuits*", Microelectronics & Reliability, 2007, Vol. 47, No. 8, pp. 1288-1295, ISSN: 0026-2714, citira se

1. Ilić, T., **Litovski, V.,** Litovski, I., Stojilković, S., "*Computationally Efficient Large-Change Statical Analysis Of Linear Electronic Circuits*", Microelectronics and Reliability, Vol. 40, 2000, pp. 1023-38.
2.

Lxiii) U radu: Zhuang, H., He, F., Lin, X., Zhang, L., Zhang, J. Zhang, X., and Chan, M., „*A Web-Based Platform for Nanoscale Non-Classical Device Modeling and Circuit Performance Simulation*", 2009 International Conference on Web Information Systems and Mining, citira se

1. Anđelković, B., Dimitrijević, M.,, and **Litovski, V.,** "Using Grid Computing in Parallel Electronic Circuit Simulation," Electronics' 2007, Sozopol, Bulgaria, September 2007, book 4, pp. 109-114.
2. Ovaj se rad nudi i na "The MIT Press Beowulf Cluster Computing 2" stranici: http://www.toodoc.com/The-MIT-Press-Beowulf-Cluster-Computing-2-pdf.html

Lxiiii) U radu: R., Balado, L., and Figueras, J., » *Quiscent defective behaviours of analog multiplexers*", Proc. of the XVII Conference on design of circuits and integrated Systems, Santander, Spain, Nov. 2002, pp. 333-338, citira se

1. Janković, S., Maksimović, D., Petković, P., **Litovski, V.**, *"Testable Design Of Digital ASIC With Embedded Analog Multiplexers"*, 21st Int. Conf. on Microelectronics, MIEL '97, Vol. 2, Niš, Sep., 1997, pp. 779-782.
2.

Lxv) U radu: Ruey-Kuen Perng, Tien-Hsiung Weng, Kuan-Ching Li, "*On Performance Enhancement of Circuit Simulation Using Multithreaded Techniques*,", 12th International Conference on Computational Science and Engineering, CSE'09, Vancouver, Canada, 2009, Vol. 1, pp.158-165, citira se

1. Anđelković, B., **Litovski, V. B.,** and Petković, P., «*Implementation and performance analysis of parallel circuit simulator on BEOWULF cluster*», 51. Konferencija Za Elektroniku, Telekomuniklacije, Računarstvo, Automatiku i Nuklearnu Tehniku, ETRAN, Herceg Novi, 04-08 Jun, 2007, Rad. EL1.6

Lxvi) na web stranici Pdfgeni.com, u okviru teme "electronic circuit analysis and design" http://www.pdfgeni.com/book/electronic-circuit-analysis-and-design-pdf.html, nudi se

1. Savić, M., **Litovski, V**., "*Frequency Domain Electronic Circuit Analysis in an Object Oriented Environment*", Proc. of the 11th Int. Scientific and Appl. Sci. Conf. of Electronics ET2002, Sep., 2002, Sozopol, 2002. Vol. 2, pp. 65-70.

Lxvii) u radu: 16. Liao, W., Tian, F., and Liu, J., "Efficient fault diagnosis method in nonlinear circuits based on neural network", Computer Engineering and Applications, Vol 45, No.19, 2009, pp. 228-231, citira se:

1. Milovanović, D., **Litovski, V.**, *"Fault Models Of CMOS Transmission Gate"*, International Journal of Electronics, ISSN 0020-7217, Vol. 71, No. 4, May, 1991, pp. 675-683.
2.

Lxviii) u radu: priem, f., calu, j. and de craemer, r., "Towards the integration of course modules of different european institutions of higher education into a multimedia learning platform", Annual Journal of Electronics, 2009, ISSN 1313-1842, citira se

1. [2] V. Litovski, S. Lazovic. "*Basic Electronics*", Cuperac Plavi, Nis.

Lxix) Rad prof. Litovskog koji je najviše citiran je: Raković, B.D., and Litovski, V.B., "*Least-squares monotonic low-pass filters with sharp cutoff*", Electronic Letters, Vol. 9, No. 4, pp.75-76, 1973. Ukupno je u međunarodnim časopisima citiran 15 puta, prvi put 1974., a zadnji 2000. god.

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4. Inženjerske realizacije

Oblast istraživanja kojom se bavi Prof. Litovski, projektovanje integrisanih kola, izabrana je na inicijativu Elektronske industrije i Republičkog ministarstva za Nauku (tada Zajednice) daleke 1978. god. Od tog vremena do danas uz stalnu podršku Elektronske industrije,

Ministarstva za nauku, JNA, Saveznog ministarstva za razvoj, Zavoda za međunarodnu saradnju Srbije i Elektronskog fakulteta u Nišu beleži se uzlazna linija karakterisana stalnim uspesima i novim naučnim rezultatima. Samo u 1997. godini, u okviru LEDA koju vodi Prof. Litovski, isprojektovana su tri integrisana kola i dobijeni odgovarajući uzorci. Mada nije direktno eksplicirano, sva tri pomenuta projekta imaju za cilj stvaranje uslova za razvoj integrisanih kola koja će biti ugrađena u postojeće proizvode domaće industrije. Smatramo da je ovaj uspeh od izuzetnog značaja za regenerisanje svih znanja i aktivnosti iz ove oblasti posle skidanja sankcija.

Za ime prof. Litovskog vezuje se i projektovanje prvog srpskog integrisanog kola (u saradnji Elektronskog Fakulteta, "Ei Mikroelektronike" i "Rudi Čajaveca" iz Banja Luke) kao i prvog analognog integrisanog kola (u saradnji sa Univerzitetom Middlesex iz Londona).

Privatni savetnik William Lurie, iz Bocca Raton-a (21061 Cottonwood Drive), Florida 33428, USA je, u ranim osamdesetim godinama, razvio proizvodnju telekomunikacionih filtara čiji su projekti bili direktno uzeti iz radova prof. Litovskog.

Prof. Litovski je do sada rukovodio nizom strateških istraživačkih projekata koji su bili finansirani od strane Republičkog Ministarstva za Nauku, Saveznog Ministarstva za Nauku i Razvoj i od JNA.

Spisak najvažnijih projekata bio bi sledeći:

1. Period 1982-1985.: Mikroelektronske komponente (Republika Srbija)

2. Period 1985-1990.: Poluprovodnička mikroelektronika i optoelektronika (Republika Srbija)

3. Period 1991-1993. (1994.): "Softver za automatsko projektovanje specifičnih digitalnih integrisanih kola", Savezni fond za podsticanje tehnološkog razvoja SFRJ.

4. Period 1994-99.: "Mikroelektronika, optoelektronika i mikrosistemske tehnologije", podprojekt: "Simulacija projektovanje i testiranje elektronskih kola i sistema". (Republika Srbija)

5. Period 2002-2004.: Sifra projekta: IT.1.02.0075.A, "Projektovanje, testiranje i eko-projektovanje elektronskih kola i sistema" ("Design, Testing and Eco-design of Electronic Circuits and Systems") (Republika Srbija).

6. Period 2005-2008, vodi projekt šifriran kao 232014, pod naslovom "Sistem za merenje i korekciju faktora snage i izobličenja elektronskih uređaja ", koji finansira Ministarstvo Nauke i Zaštite Životne Sredine Srbije.

Projekti pod rednim brojem 1, 2 i 4 okupljali su praktično sve istraživačke organizacije iz oblasti mikroelektronike u Srbiji.

U tri navrata, 1989., 1995. i 1999. god. prof. Litovski bio je angažovan na istrazivačkim projektima koje je finansirala Britanska vlada, a koji su se realizovali na univerzitetu u Sautemptonu (*www.soton. ac.uk/~newrep/vol14/no9people.html*). U prvom slučaju, 1989.-1991, (Alis No. 245, Belgrade), radilo se o uspostavljanju saradnje tzv. Academic Link, a finansijsku podršku je realizovao Britanski Savet u Beogradu. U drugom slučaju, 1995.-1995. god. (Istraživački projekt „Mixed signal fault modelling and simulation“,Grant ref. No. GR/K54129, 12 June 2005), kao i u trećem, 1999.-2000. god. (Istraživački projekt „Modelling and Simulation of Actuators in Implanted Hearing Aids Using Neural networks“, Grant no. GR/M85531, 02 July 1999), finansijsku podršku je realizovao EPSRC (Electronics and Physics Research Council). U periodu 2000.-2002. god. realizovan je projekt razvoja digitalnih integrisnih kola velike brzine sa temama: “Low bit High Speed BOSA DSM”, “Evaluation and Design of a High Frequency Low Pass Oversampling DAC” i “Band Pasas Oversampling AD Converter”. Prof. Litovski rukovodio je Niškim delom projekta.

U periodu 2001-2006, Prof. Litovski angažovan je ka rukovodilac podprojekta, na projektu ISSN koji u okviru Pakta o stabilnosti Jugoistočne Evrope finansira Nemački zavod za medjunarodnu akademsku saradnje (DAAD) na kome učestvuju istraživači sa univerziteta u Ilmenau (Nemačka), Sofiji, (Bugarska) i Skoplju (Makedonija). (Izveštaj DAAD:

Stabilitaetspakt fuer Suedosteuropa DAAD-Sonderprogramm "Akademischer Neuaufbau Suedeuroa", Bonn, 23.06.2001.) *www.daad.de/magazin/stipendien_programme/de_hochschulen/stabilitaet projekt_mathe.rtf*. U okviru ovog projekta na Elektronskom fakultetu instaliran je prvi klaster računara koji formira osmoprocesorski superračunar.

U periodu 2006. god. i nadalje Prof. Litovski vodi niški deo evropskog FP6 projekta: "SEEGIRD 2 - South Eastern European GRid-enabled eInfrastructure Development 2", koji od maja 2008 prerasta u "SEE-GRID eInfrastructure for regional eScience – SEE-GRID-SCI"

5. Spisak publikacija

Monografije

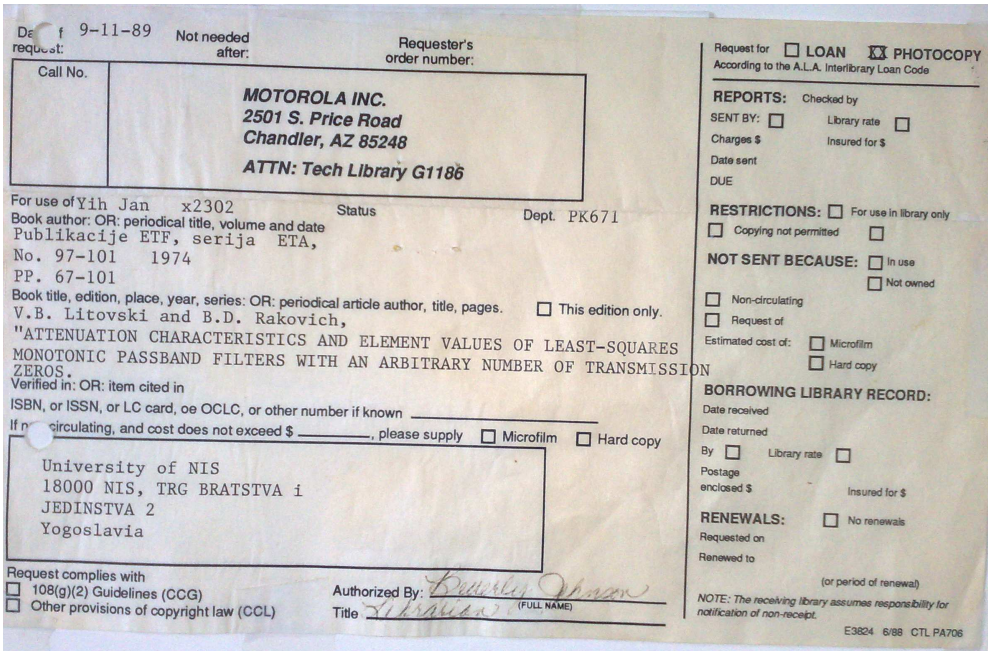
1. **Litovski, V.**, *"Automatizacija projektovanja integrisanih kola"*, u "MIPRO'88 Mikroelektronički sklopovi-principi rada i projektiranja", pod redakcijom prof. Petra Biljanovića, Rijeka, Maj, 1988.
2. **Litovski, V.**, *"Logička simulacija"*, u monografiji: "Projektovanje VLSI, I deo", Nauka, Beograd, 1991, pp. 106-181.
3. Radenković,T., Radenković, Z., **Litovski, V.**, *"Integrisani softverski paket za projektovanje gejtovskih matrica (ISPGM)"*, u monografiji "Projektovanje VLSI, I deo", Nauka, Beograd, 1991, pp. 411-481.

Pregledni članci u časopisima međunarodnog značaja

1. Damnjanović, M., **Litovski, V.**, *"A Survey Of Routing Algorithms In Custom IC Design"*, Journal of Semicustom ICs, (ISSN 0026-2692, Microelectronics Journal (Incorporating Journal Of Semicustom Ics)), Vol. 7, No.2, December, 1989, pp. 10-19.

Radovi u časopisima međunarodnog značaja

1. Raković, B.D., **Litovski, V.**, *"Least-Squares Monotonic Lowpass Filters With Sharp Cutoff"*, Electronic Letters, ISSN: 0013-5194, Vol. 9, No. 4, 1973, pp. 75-76.
2. Raković, B.D., **Litovski, V.**, *"Monotonic Passband Low-Pass Filter With Chebyshev Stopband Attenuation"*, IEEE Trans.on Acoustics, speech,and signal processing, ISSN**:** 0096-3518, Vol. ASSP-22, 1974, pp. 39-44.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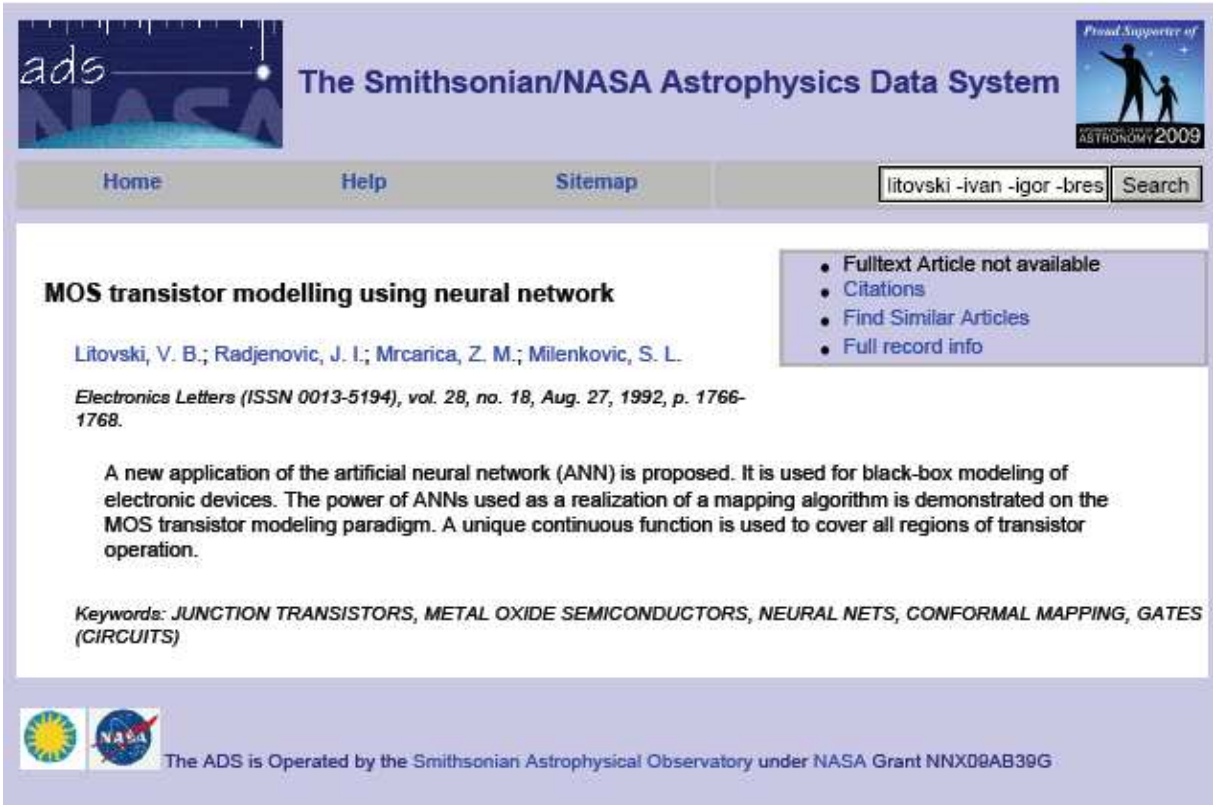
3. **Litovski, V.**, Raković, B.D., *"Attenuation Characteristics And Element Values Of Least-Squares Monotonic Passband Filters With An Arbitrary Number Of Transmission Zeros"*, Publikacije Elektrotehničkog fakulteta, Serija ETA, No. 97-101, 1974, pp. 67-101.
4. **Litovski, V.**, Lazović, S., *"Design Of General Stopband Lowpass Filters With Equiripple Passband Response"*, Publikacije Elektrotehničkog fakulteta, Serija ETA, No. 102-106, 1974, pp. 45-52.
5. **Litovski, V.**, *"Synthesis Of Monotonic Passband Sharp Cutoff Filters With Constant Group Delay Response"*, IEEE Trans. on Circuits and Systems, ISSN: 1549-8328, Vol. CAS-26, No. 8, 1979, pp. 597-602.
6. **Litovski, V.**, Milovanović, D., *"New Solution For The Ideal Filter Approximation Problem"*, IEE Proceedings, Pt. G. , ISSN, 0143-7089,Vol. 130, No. 4, August, 1983, pp. 161-163.
7. Glozić, D., **Litovski, V.**, Bayford, R., *"ASCOTA3 - A New Automatic Hierarchical CMOS Opamp Synthesizer"*, Facta Universitatis, series: Electronics and Energetics, Vol. 4, No. 1, 1991, pp. 81-105.
8. Milovanović, D., **Litovski, V.**, *"Fault Models Of CMOS Transmission Gate"*, International Journal of Electronics, ISSN 0020-7217, Vol. 71, No. 4, May, 1991, pp. 675-683.
9. Radenković, Z., Radenković, T., Stojilković, S.M., **Litovski, V.**, *"A Knowledge - Based Layout Compaction Procedure"*, Microelectronics Journal, Vol. 23, No. 2, April, 1992, pp. 121-132.



10. **Litovski, V.**, Rađenović, J., Mrčarica, Ž., Milenković, S., *"MOS Transistor Modelling Using Neural Network"*, Electronics Letters, Vol. 28, No. 18, Avgust, 1992, pp. 1766-1768.
11. Mrčarica, Ž., **Litovski, V.**, *"A New Ideal Switch Model For Time-Domain Circuit Analysis"*, International Journal of Electronics, ISSN 0020-7217, Vol. 74, No. 2, 1993, pp. 241-250.
12. Petković, P., **Litovski, V.**, *"New Generalized Approach To The Macromodeling Of Digital Structures"*, Electron Technology, Vol. 26, No. 2/3, Warsaw, Poland, 1993, pp. 53-75.
13. **Litovski, V.**, Mrčarica, Ž., *"Macromodeling With Spice's Nonlinear Controlled Sources"*, IEEE Circuits and Devices Magazine, Vol. 9, No. 6, November, 1993, pp. 14-17,51.
14. Milovanović, D., **Litovski, V.**, *"Fault Models Of CMOS Circuits"*, Microelectronics and Reliability, Vol. 34, No. 5, May, 1994, pp. 883-896.
15. Glozić, D., **Litovski, V.**, Bayford, R., *"ASCOTA3 ADIL: A New Reconfigurable CMOS Analogue VLSI Design Framework"*, Microelectronics Journal, Vol. 25, No. 5, Aug., 1994, pp. 335-351.
16. Milenković, S., **Litovski, V.**, *"New Analytical Procedure For Automatic Cell Placement In Gate-Arrays"*, IEE Proceedings part G, Circuits Devices System, Vol. 141, No. 6, Dec., 1994, pp. 476-482.
17. Petković, P., Stojilković, S., **Litovski, V.**, "*New Factorization Algorithm For Symbolic Circuit Analysis*", Electronic Letters, Vol. 31, No. 13, 22. Jun, 1995, pp. 1026-1027.
18. Mrčarica, Ž., Vujanić, A., Detter, H., **Litovski, V.**, "*Simulation Of Micromechanical Systems*", 6th International Journal of Theoretical Electrotechnics, Thessaloniki, Greece, Sep., 1996, pp. 141-148.
19. Rađenović-Mrčarica, J., Mrčarica, Ž., Detter, H., **Litovski, V.**, *"Neural Network Visual Recognition For Automation Of The Microelectromechanical Systems Assembly"*, International Journal on Neural Systems, Vol. 8, No. 1, Feb., 1997, pp. 69-79.
20. Petković, P., Milovanović, D., **Litovski, V.**, *"Symbolic Fault Modelling And Test Generation Of MOS Circuits"*, Microelectronics and Reliability, Vol. 37, No. 1, 1997, pp. 137-157.

21. Mrčarica, Ž., **Litovski, V.**, Detter, H., *"Modelling And Simulation Of Microsystems Using Hardware Description Language"*, Research Journal on Microsystem Technologies, Vol. 3, No. 2, Feb., 1997, pp. 80-85.
22. **Litovski, V.**, Mrčarica, Ž., Ilić, T., *"Simulation Of Non-Linear Magnetic Circuits Modelled Using Artificial Neural Network"*, Journal Simulation Practice and Theory, Vol. 5, No. 6, 1997, pp. 553-570.
23. Maksimović, D., **Litovski, V.**, *"Logic Simulation Based Method For Digital CMOS VLSI Circuits Power Estimation "*, 7th International J. Of Theoretical Electrotechnics, Join to ISTET '97, Cottbus, 1999, pp. 40-43.
24. **Litovski, V.**, Dimić, Ž., Damnjanović, M., Mrčarica, *Ž., "Electronic Circuit Simulatoion In A Mixed-Language Environment*", Miroelectronics Journal, Vol. 29, No. 8, 1998, pp. 553-558.
25. Maksimović, D., **Litovski, V.**, "*Tuning The Logic Simulator For Timing Analysis*", Electronics Letters, Vol. 35, No. 10, 13th May, 1999, pp. 800-802.
26. Mrčarica, Ž., Ilić, T., **Litovski, V.**, "*Time-Domain Analysis Of Nolinear Switched Networks With Internally Controlled Switches*", IEEE Transactions on Circuits and Systems I, Vol. 46, No. 3, March, 1999, pp. 373-378.
27. Jakovljević, M., Mrčarica, Ž., Fotiu, P., Detter, H., **Litovski, V.**, "*Transient Electro-Thermal Simulation Of Microsystems With Space-Continuous Thermal Models In Analogue Behavioural Simulator*", Microelectronics and Reliability, Vol. 40, No. 3, March 2000, pp. 507-516.
28. Ilić, T., **Litovski, V.,** Litovski, I., Stojilković, S., "*Computationally Efficient Large-Change Statical Analysis Of Linear Electronic Circuits*", Microelectronics and Reliability, Vol. 40, 2000, pp. 1023-38.
29. **Litovski, V.,** Maksimović, D., and Mrčarica, Ž., "*Mixed-signal modelling with AleC++: Specific features of the HDL*", Simulation Practice and Theory, Vol. 8, 2001, pp. 433-449.
30. Jakovljevic M., Fotiu P.A., Mrčarica Ž., **Litovski V.** and Detter H., "*Electro-thermal simulation of microsystems with mixed abstraction modelling* " Microelectronics Reliability, Volume 41, Number 6, June 2001 , pp. 823-835(13), Elsevier.
31. Damnjanović, M., Anđelković, B., **Litovski**, V., "*VHDL-AMS Compiler for Alecsis Simulation Environment*", Electronics, Vol. 6, No. 2, December 2002, pp. 6-11.
32. Stefanović, D., Kayal, M., **Litovski**, V.B., "*An Interactive Knowledge Based Analog Design Approach*", Electronics, Vol. 6, No. 2, December 2002, pp. 22-25.
33. Janković, S., Maksimović, D., **Litovski**, **V.B.**, "*Modern 32-bit Microcontroller Characteristics and Automotive Applications*", Electronics, Vol. 6, No. 2, December 2002, pp. 62-76.
34. Milojković, J., **Litovski, V. B.,** "*Eco-Design in Electronics – The State of the Art*", Facta Universitatis, Series: Working and Living Environmental Protection, Vol. 2, No. 2, 2002, pp. 87-100.
35. **Litovski, V.**, "*New Methods in Modeling and Simulation of Electronic Circuits and Systems*", Scientific Review, No. 29-30, 2001-2002, pp.189-207.
36. Maksimović, D., **Litovski, V.**, "*Logic simulation methods for longest path delay estimation*", IEE Proceedings Computers and Digital Techniques, Vol. 149, No. 2, 2002, pp. 53-59.
37. Savić, M., **Litovski, V.,** "*Behavioral object-oriented frequency domain electronic simulation*", Simulation News Europe, No. 38/39, December 2003, pp. 38-39.
38. Andrejević, M., **Litovski, V.,** "*Electronic Modelling Using ANNs For Analogue and Mixed-Mode Behavioural Simulation*", Journal of Automatic Control, University of Belgrade, Vol. 13, No. 1, 2003, pp. 31-37.

39. **Litovski, V. B.**, Andrejević, M., Petković, P., Damper, R., "*ANN Application to Modelling of the D/A and A/D Interface for Mixed-Mode Behavioural Simulation*", Journal of Circuits, Systems and Computers, Vol. 13, No. 1, February 2004, pp. 181-192.
40. **Litovski,V.,** Litovski, I., and Zwolinski, M., "*Concurrent analogue fault simulation, the equation formulation aspect*", Int. Journal of Circuit Theory and Aplications, Vol. 32, December 2004, pp. 467-507.
41. Andrejević, M., **Litovski, V.,** and Zwolinski, M., "*Black-Box Application in Modeling of Micro-electro-mechanical Systems*", Electronics, Vol. 8, No. 2, December 2004, pp. 27-30.
42. Dimitrijević, M., and **Litovski, V**., "*Implementation of the component characteristic curve tracer using PC-based acquisition card*", Electronics, Vol. 8, No. 2, December 2004, pp. 35-38.
43. **Litovski, V**., Andrejević, M., and Zwolinski, M., "*Acceleration of MEMS fault simulation using ANNs*", Electronics, Vol. 8, No. 2, December 2004, pp. 49-53.
44. Milenković, S., and **Litovski, V.**, "*Passive image rejection filters optimized for telecommunication application*", Electronics, Vol. 8, No. 2, December 2004, pp. 54-63.
45. Savić, M., and **Litovski, V.,** "*Bandgap voltage reference in CMOS*", Electronics, Vol. 8, No. 2, December 2004, pp. 68-70.
46. Savić, M., Mrčarica, Ž., and **Litovski, V.**, "*Ideal Switch Model Speeds Up the Switched Circuits Simulation*", WSEAS Transactions on Circuits and Systems, Vol. 4, No. 11, November 2005, pp. 1657-1663.
47. Savić, M. and **Litovski, V.**, "*Comparison of ideal and SPICE switches for electronic circuit simulation*", Simulation News Europe, Issue 43, July 2005, pp. 17-19.
48. Savić, M. **Litovski, V.**, and Mrčarica, Ž., "*Electronic circuit simulation with ideal switches*", HAIT Journal of Science and Engineering, B 2, No. 3-4, 2005, pp. 476-495.
49. Milojković, J., and **Litovski, V.**, "*Concepts of computer take-back for sustainable end-of-life*", Facta Universitatis, Series: Working and Living Environmental Protection, Vol. 2, No. 5, 2005, pp. 363-372.
50. **Litovski, V.,** Andrejević, M., and Zwolinski, M. "*Analog electronic circuit diagnosis based on ANNs* ", Microelectronics Reliability, Vol. 46, No. 8, 2006, pp. 1382-1391.
51. **Litovski, V**., Savić, M., and Mrčarica, Ž., " *Implementation Of Ideal Switch Model Cuts Significantly Simulation Time*", IEEE Circuits and Devices Magazine, Vol. 22, No. 4, July/August 2006, pp. 16-22.
52. Milojković, J., and **Litovski, V.,** „*Take back concepts and end-of-life management of power electrical components*", Electronics, Vol. 10, No. 2, December 2006, pp. 59-63. YU ISSN 1450-5843
53. Anđelković, B., **Litovski, V.,** and Zerbe, V., "*Mission Level Modeling And Simulation Language For Mixed-Signal System-On-A-Chip Design*", Journal of Circuits, Systems and Computers (World Scientific Publishing Company), Vol. 16, No. 1, February 2007, pp. 15-28.
54. Anđelković, B., and **Litovski, V.,** „*Parallel transistor level simulation based on parallel equation formulation implementated on Beowulf cluster*", Simulation News Europe, Vol. 17, No. 3/4, December 2007, pp. 55-58. ISSN 0929-2268.
55. Dimitrijević, M., and **Litovski,V.B**., „*Implementation of compact switching power supply with high power factor*", Electronics, Vol. 11, No. 1-2, December 2007.ISSN 1450-5843.
56. Sokolović, M., **Litovski, V.,** Zwolinski, M., "*New Concepts of Worst Case Delay and Yield Estimation in Asynchronous VLSI Circuits***",** Microelectronics Reliability, ISSN 0026-2714, February, 2009, Vol. 49, No. 2, pp. 186-198.
57. **Litovski, V. B.,** and Petkovic, P. M., "*Why does the grid needs cryptography?*" Electronics, ISSN: 1450-5843, Vol. 13, No. 1, June 2009, pp. 30-36.

58. Sokolović M., and **Litovski, V., "***Statistical timing analysis of asynchronous circuits using logic simulator***",** Electronics, ISSN: 1450-5843, Vol. 13, No. 1, June 2009, pp. 37-42.
59. Sokolović,M., **Litovski, V.**, and Zwolinski, M., "*Efficient and realistic statistical worst case delay computation using VHDL*", Electrical Engineering, ISSN: 0948-7921, DOI 10.1007/s00202-009-0133-y**,** Volume 91, Numbers 4-5 / December, 2009, pp. 197-210
60. Milojković, J, and **Litovski, V.B.,** „*Dynamic Short-Term Forecasting Of Electricity Load Using Feed-Forward ANNs*", International Journal of Engineering Intelligent Systems for Electrical Engineering and Communication, ISSN 1472-8915, Vol. 17, No. 1, March 2009.
61. Milojković, J., Litovski, V., „*Short Term Forecasting in Electronics***",** International Journal of Electronics, ISSN 0020-7217, 2010, accepted.

36 sa SCI liste

Radovi u domaćim časopisima

1. **Litovski, V.**, *"Filtri sa maksimalno zaravnjenom karakteristikom grupnog kašnjenja i jedna nova klasa filtara sa dobrim grupnim kašnjenjem"*, Naučni podmladak, Vol. 2, 1970, pp. 115-126.
2. **Litovski, V.**, *"Granično monotona amplitudna karakteristika sa konačnim nulama prenosa i maksimalnim nagibom na granici propusnog opsega"*, Tehnika (Elektrotehnika), Vol. 26, No. 2, 1977, pp. E1-E3.
3. **Litovski, V.**, Petrović, G., *"Sinteza filtarske ćelije drugog reda sa proizvoljnim rasporedom nula prenosa"*, Tehnika (Elektrotehnika), Vol. 27, No. 7-8, 1978, pp. E1-E3.
4. Lazović, S., **Litovski, V.**, *"Karakteristike niskofrekventnih monotonih filtara za linijske skretnice"*, Zbornik radova Saobraćajnog fakulteta, Vol. 28, No. 4, 1979, pp. 49-93.
5. **Litovski, V.**, Mitić, P., *"Sinteza prenosnih funkcija selektivnih filtara propusnika opsega s linearnom faznom karakteristikom"*, Tehnika (Elektrotehnika), Vol. 29, No. 1, 1980, pp. E1-E6.
6. **Litovski, V.**, Jevtić, M., Pantić, S., *"Uticaj nesavršenosti operacionih pojačavača na karakteristike niskopropusnih filtara"*, Tehnika (Elektrotehnika), Vol. 29, No. 10, 1980, pp. E7-E12.
7. **Litovski, V.**, Stanković, T., *"Simulacija prelaznih režima u električnim kolima sa magnetima sa pokretnom kotvom"*, Elektronika (Nauka i praksa), Vol. 1, Br. 1, 1981, pp. 16-21.
8. Milovanović, D., **Litovski, V.**, *"Fazni korektori u električnim filtrima neminimalne faze"*, Tehnika (Elektrotehnika), Vol. 31, No. 6, 1982, pp. 1025-1028.
9. Stanojević, S., **Litovski, V.**, *"Simbolička analiza električnih kola"*, Tehnika (Elektrotehnika), Vol. 31, No. 12, 1982, pp. 1895-1989.
10. Damnjanović, M., **Litovski, V.**, *"Realizacija jednog algoritma za projektovanje veza u integrisanim kolima"*, Automatika, Zagreb, Vol. 23, No. 1-2, 1982, pp. 47-53.
11. Milenković, S., **Litovski, V.**, *"Kolo za trostepenu regulaciju boje tona"*, Naučni podmladak, Vol. XVIII, No. 1-2, Univerzitet u Nišu, 1986.
12. **Litovski,V.**, *"LIFT - računarski program za analizu linearnih elektronskih kola "*, Elektrotehniški vestnik, Ljubljana, Vol. 53, No. 4-5, 1987, pp. 287-293.
13. **Litovski, V.**, Milenković, S., Milićević, M., *"Generisanje inicijalnog razmeštaja u gejtovskoj matrici GEM21"*, Tehnika (Elektrotehnika), Vol. 36, No. 10, 1987, pp. 957-960.
14. **Litovski, V.**, Petković, P., Milenković, S., *"Analiza MOS integrisanih kola upotrebom programa MOST II"*, Elektronika (nauka i praksa), Vol. 8, No. 1/2, Jun, 1988, pp. 3-14.
15. Damnjanović, M., **Litovski, V.**, *"Jedno rešenje povezivanja u gejtovskoj matrici GEM 21"*, Elektrotehnika (Tehnika), Vol. 37, No. 3, 1988, pp. 337-340 (e1-e4).
16. Ilić, S., **Litovski, V.**, *"Simulacija tiristorskog invertora u kolu za generisanje visokog napona u rentgenskim uredjajima"*, Elektrotehnika (Tehnika), Vol. 37, No. 2, 1988, pp. 221-227 (e13-e19).

17. Janićijević, I., Radenković, Z., Janković, T., **Litovski, V.**, *"Experiences With Gks-Equivalent Software Development For 16-Bit Machines"*, ([tampano u zborniku - "Automatika-appendix" posle recenzije radova sa Konf.: "The Third Int. Conf. on Computer Graphics"), 22-24 june, 1988, Automatika, Zagreb, Vol. 29, No. 1-2, pp. a.357-a.362.
18. Mrčarica, Ž., **Litovski, V.**, Petković, P., *"Izbor modela kratkokanalnog MOS tranzistora za simulaciju elektronskih kola"*, Tehnika (Elektrotehnika), Vol. 40, No. 5-6, 1991, pp. e1-e5.
19. Glozić, D., **Litovski, V.**, *"ASCOTA2 - program za automatsko projektovanje CMOS operacionih pojačavača"*, Tehnika (Elektrotehnika), Vol. 40, No. 7-8, 1991, pp. e1-e7.
20. Radenković, Z., **Litovski, V.**, *"Z-R kompakcija podržana znanjem"*, Tehnika (Elektrotehnika), Vol. 42, No. 4, 1993, pp. e6-e11.
21. Zarković, K., Ranđelović, Z., Milenković, S., Novaković, M., Jovanović, Lj., **Litovski, V.**, *"JUDGE - Jacquard Developing Environment (Editor)"*, Tekstilna industrija, No. 3-4/97, Beograd, 1997.
22. Janković, S., Maksimović, D., Živković, V., Petković, P., **Litovski, V.**, "*Testabilno digitalno integrisano kolo specifične namene sa ugradjenim analognim multiplekserom*", Elektronika, Vol. 1, No. 1, Decembar, 1997, pp. 56-60.
23. Maksimović, D., Janković, S., **Litovski, V.**, "*Alecsis: Modeliranje i predikcija perfomansi digitalnih VLSI kola*", Tehnika (Elektrotehnika), Vol. 47, No. 2, 1998, pp. E6-E20.
24. Maksimović, D., **Litovski, V.**, "*Analiza topoloških kašnjenja u digitalnim kolima pomoću logičkog simulatora*", Tehnika (Elektrotehnika), Vol. 48, No. 2, 1999, pp. E1-E13.
25. Maksimović, D., Panić, V., Zarković, K., Petković, Z., Milovanović, D., Topisirović, D., Litovski, V., "*Implementacija digitalnih elektronskih kola primenom boundary scan standarda*", Tehnika (Elektrotehnika), Vol. 50, 2001, pp. E7-E15.
26. Andrejević, M., **Litovski, V.**, "*Primena veštačkih neuronskih mreža za modelovanje reaktivnih nelinearnih dvopola*", Tehnika (Elektrotehnika), Vol. 51, No. 4-5, Maj 2002, pp. E1-E11.
27. Stefanović, D., Kayal M., **Litovski V.**, "*Proceduralno projektovanje analognih CMOS integrisanih kola na primeru Milerovog operacionog pojačavača*", Tehnika (Elektrotehnika), Vol. 52, No. 2, 2003, pp. 8-17.
28. Jovanović. B., Damnjanović, M., i **Litovski, V.**, «*Square Root on Chip*", ETF Journal of Electrical Engineering, A Publication of the EE Department, University of Montenegro May 2004 Vol.12 No.1 YU ISSN: 0353-5207
29. Dimitrijević, M., i **Litovski V.**, "*Laboratorija za elektroniku podržana računarskom mrežom*", Tehnika (Elektrotehnika), Vol. 55, No. 3, 2006, pp. E.3-E.9.
30. Milojković, J., i **Litovski V.**, "*Postupci predviđanja količina elektronskog otpada od računara*", Tehnika (Elektrotehnika), Vol. 56, No. 1, 2007, pp. E.7-E.16.

Radovi po pozivu na međunarodnim Konferencijama

1. **Litovski, V.**, *"An Integrated System For Gate-Array Design"*, Proc. of the Int. Symposium: Hybrid and Semiconductor Technology, Gate-Arrays and Semiconductor Lasers, Sozopol, May, 1988, pp. 25-67.
2. Damnjanović, M., **Litovski, V.**, "*Routing Algorithms In Custom Ic Design*", Proc. of the 2nd Hungarian Custom Circuits Conference, CCC 89., Szeged, 10-12 Maj, 1989, pp. 83-111.
3. **Litovski, V.**, *"New Results In Integrated Software Development For Gate-Array Design"*, Proc. of the 3rd MidEuropean Custom Circuit Conference, Sopron, 21-24 April, 1991, pp. 69-83.
4. **Litovski,V.**, *"New Tehnologies In Integrated Circuits Design"*, 2nd Serbian Conference on Microelectronics and Optoelectronics, MIOPEL '93, Niš, 26-28 Oktobar, 1993, pp. 383-399.

5. Zwolinski, M., **Litovski, V.**, *"Hybrid Simulation: The State-Of-The-Art"*, 2nd Serbian Conference on Microelectronics and Optoelectronics, MIOPEL '93, Niš, Srbija, 26-28 Oktobar, 1993, pp. 375-382.
6. Milenković, S., **Litovski, V.**, Obradović, Z., *"A New Adaptive Move Type Selection In Simulated Annealing"*, 15-16 Int. Anual School on Semiconductor and Hybrid Technologies, 1992-93, Sozopol, May, 1994, pp. 22-31.
7. Pantić, D., Milenković, S., Trajković, T., **Litovski, V.**, Stojadinović, N., *"Inverse Modeling Of Semiconductor Manufacturing Processes"*, 20th Int. Conference on Microelectronics MIEL '95, Vol. 1, Niš, 12-14 Sep., 1995, pp. 321-326.
8. **Litovski, V.**, Ranđelović, Z., Damnjanović, M., *"A Routing In Standard Cells"*, 20th International Conference on Microelectronics MIEL '95, Vol. 2, Niš, 12-14 Sep., 1995, pp. 461-466.
9. Petković, P., Milovanović, D., **Litovski, V.**, *"Symbolic Function Extraction And Fault Modelling Of MOS Circuits"*, 20th Int. Conference on Microelectronics MIEL '95, Vol. 2, Niš, 12-14 Sep., 1995, pp. 473-478.
10. Andrejević, M., **Litovski, V.,** "*Electronic Modelling Using ANNs For Analogue and Mixed-Mode Behavioural Simulation*", Proc. of Neurel 2002, 2002, pp. 113-118.
11. Sokolović, M., Zwolinski, M., and **Litovski, V**., "*New Concepts of Worst-case Delay Evaluation in Asynchronous VLSI SoC*", PROC. 26th International Conference On Microelectronics (MIEL 2008), Niš, Serbia , 11-14 May, 2008, pp. 377-385. Invited paper

Radovi po pozivu na domaćim Konferencijama

1. Zarković, K., Milenković, S., Glozić, D., **Litovski, V.**, *"Novi rezultati u primeni neuronskih mreža za modeliranje i simulaciju elektronskih kola"*, 3rd Seminar on Neural Network Applications in Electrotechnics NEUREL-95, 29-30 Sep., 1995, pp. 108-116.
2. **Litovski, V.**, Aleksić, D., Milenković, S., "*Simulacija računarskih mreža*", Šesnaesti Simp. o novim tehnologijama u poštanskom i telekomunikacionom saobraćaju, Beograd, 1998.
3. **Litovski, V. B**., «*Razvoj sekcije "Elektronika" u okviru konferencije ETRANa - prvih 50 godina*» L Konferencija ETRANa, Beograd, Juni 2006. god., pp. EL, 1, 5-8.

Radovi na međunarodnim Konferencijama

1. Lazović, S., **Litovski, V.**, *"A New Method Of Band-Pass Allpass Network Synthesis For Compression"*, Proc. of the II International Symposium on Network Theory, Herceg-Novi, 1971, pp. 275-284.
2. **Litovski, V.**, *"Lowpass Filter Design Using Complex Transmission Zeros"*, Proceedings of the 23. Intern. Wiss. Koll. TH, Ilmenau, 1978, pp. 29-32.
3. **Litovski, V.**, *"Computer And Electronic Simulation Of Ring Waterwork Systems"*, Proceedings of the 24. Intern. Wiss. Koll. TH, Ilmenau, 1979, pp. 133-136.
4. **Litovski, V.**, *"Transient Simulation In Circuits With MOS Transistors"*, Proc. of the 27. Intern. Wiss. Koll. TH, Ilmenau, 1982, pp. 237-240.
5. **Litovski, V.**, Petković, P., *"Time Domain Temperature Dependence Simulation Of MOS Electronic Circuits"*, Proc. of the 6th International conference on computers in design engineering, CAD84, Brighton, April, 1984, pp. 61-66.
6. **Litovski, V.**, Pantić, S., *"LANA: Fortran Subroutine For MOS-Transistor-Model Implementation In Circuit-Analysis Program"*, Proc. of the 7th European conf. on Electrotechnics, EUROCON 86, Paris, april, 1986, pp. 436-441.
7. Petković, P., **Litovski, V.**, *"Macromodeling And Macroanalysis Of CMOS LSI Electronic Circuits"*, Proc. of the Conf. on VLSI and Computers, COMPEURO 87, Hamburg, May, 1987, pp. 512-513.

8. **Litovski, V.**, Milovanović, D., Stojanović, Z., *"LOSTIN - A Computer Program For Communication With A Gate Level Logic Simulator"*, Proc. of the 32 Int. Wiss. Kolloq. der TH Ilmenau, October, 1987 , pp. 215-218.
9. **Litovski, V.**, Petković, P., *"Time Domain Black-Box Modelling Of CMOS Structures And Analog Timing Simulation"*, 3rd Annual European Computer Conf., COMPEURO '89, Hamburg, May, 1989, pp. 5.142-5.143.
10. **Litovski, V.**, Gmitrović, M., *"Interconnect Modelling And Simulation In VLSI"*, Proc. of the VII Int. Conf. on Microelectronics, MICROELECTRONICS '90, Minsk, October, 1990, pp. 21-22.
11. Damnjanović, M., **Litovski, V.**, *"Global And Detailed Automatic Routing In A Gate-Array"*, Proc. of the 35. Int. Wiss. Kolloquium, Ilmenau, 22-26 October, 1990, pp. 25-28.
12. Milovanović, D., **Litovski, V.**, *"New CMOS Transmission Gate Fault Models And Fault Simulation"*, Proc of the Int. Conf. on Concurrent Engineering and Electronic Design Automation, CEEDA '91, Poole, March, 1991, pp. 393-395.
13. Petković, P., **Litovski, V.**, *"Output Resistance Of CMOS Logic Cells"*, Proc. of the 3rd Mideuropian CCC 1991, Sopron, Hungary, April, 1991, pp. 237-244.
14. Milenković, S., **Litovski, V.**, *"Analytical Approach To The Placement Problem In Gate-Arrays"*, IEEE COMPEURO '91, Bologna, Italy, May, 1991, pp. 800-804.
15. Mrčarica, Ž., **Litovski, V.**, *"Some Considerations Of Short-Channel MOS Model Selection For An Analog Circuit Simulation Program"*, Microsystem '92, Bratislava, 17-19. November, 1992.
16. Glozić, D., **Litovski, V.**, Petković, P., *"ADIL: - Analog Design Instruction Language For More Flexible Simulation In Synthesis Process"*, EUROSIM '92, Capri, 28.9-2.10, 1992, pp. 453-458.
17. **Litovski, V.**, *"Simulated Intelligence And The Design Of Electronic Circuits"*, 37. Internationales Wissenschaftliches Kolloquium, Ilmenau, 21-24.9, 1992.
18. **Litovski, V.**, Pantić-Tanner, Z., *"Artificial Neural Network Application In Electronic Circuit Analysis"*, World Congress On Neural Networks, Portland, Oregon, 11-15 July, 1993.
19. Milovanović, D., **Litovski, V.**, Obradović, M., *"Modeling Procedures For BiCMOS Cells"*, 2nd Serbian Conf. on Microelectronics and Optoelectronics, MIOPEL '93, Niš, 26-28 Oktobar, 1993, 421-425.
20. Milovanović, D., **Litovski, V.**, *"A Review Of Fault Models Of BiCMOS Cells"*, 2nd Serbian Conf. on Microelectronics and Optoelectronics, MIOPEL '93, Niš, 26-28 October, 1993, pp. 415-420.
21. Damnjanović, M., **Litovski, V.**, *"CAD Systems Based On VHDL Description"*, 2nd Serbian Conf. on Microelectronics and Optoelectronics, MIOPEL '93, Niš, 26-28 October, 1993, pp. 443-448.
22. Petković, P., Stevanović, R., **Litovski, V.**, *"Approach To Linear Circuit Analysis"*, 2nd Serbian Conf. on Microelectronics and Optoelectronics, MIOPEL '93, Niš, 26-28 October, 1993, pp. 437-442.
23. Milenković, S., **Litovski, V.**, *"A New Adaptive Generation Strategy In Simulated Annealing"*, European Conf. in Circuit Theory and Design, ECCTD '93, Davos, 30.8-3.9, 1993.
24. Ranđelović,Z., **Litovski,V.**, *"An Application Of Hopfield-Tank's Neural Net On Chanel Routing"*, 15-16 International Annual School on Semiconductor and Hybrid Technologies, 1992-93, Sozopol, May, 1994, pp. 106-111.
25. Petković, P., **Litovski, V.**, *"Linear Circuit Analysis Based On Symbolic Algebra"*, 15-16 International Annual School on Semiconductor and Hybrid Technologies, 1992-93, Sozopol, May, 1994, pp. 112-120.

26. Milovanović, D., **Litovski, V.**, *"Logic Models Of CMOS Transmission Gate With A Floatin-Gate Transistor"*, 15-16 International Annual School on Semiconductor and Hybrid Technologies, 1992-93, Sozopol, May, 1994, pp. 126-132.
27. Maksimović, D., Glozić, D., **Litovski, V.**, *"Logic Simulation Modeling Techniques In Hybrid Simulator Alecsis2.0"*, 15-16 International Annual School on Semiconductor and Hybrid Technologies, 1992-93, Sozopol, May, 1994, pp. 133-139.
28. Milovanović, D., **Litovski, V.**, Jevtić, M., *"Fault Modeling Of MSD Flip-Flops"*, 17th Edition of Annual Semiconductor Conference, CAS '94, Proceedings Volume 2, Sinaia, 11-16 Oct., 1994, pp. 401-404.
29. Maksimović, D., Glozic, D., **Litovski, V.**, *"Discrete Event Modeling And Simulation In An Object Oriented Hybrid Simulator"*, XIV IASTED International Conference: Modelling Identification and Control, Innsbruck, Feb., 1995, pp. 103-106.
30. Ranđelović, Z., Milenković, S., **Litovski, V.**, *"Global Routing For The Standard Cell Layout"*, Annual School - 17th International Spring Seminaron Semicoductor and Hybrid Technologies 1994-1995, Sozopol, 1995, pp. 248-254.
31. Janković, S., Milovanović, D., **Litovski, V.**, *"Experiences In Using The System Magic For Designing IC"*, Annual School - International Spring Seminar on Semicoductor and Hybrid Technologies 1994-1995, Sozopol, 1995, pp. 242-247.
32. Dimić, Ž., Damnjanović, M., Glozić, D., **Litovski, V.**, *"VHDL Use For Alecsis Hybrid Simulation"*, Annual School - 17th International Spring seminar on Semiconductor and Hybrid Technologies 1994-1995, Sozopol, 1995, pp. 228-241.
33. Mrčarica, Ž., Ilić, T., Glozić, D., Detter, H., **Litovski, V.**, *"Mechatronics Simulation Using Alecsis, Anatomy Of Simulator"*, EUROSIM '95, Vienna, 1995, pp. 601-604.
34. Mrčarica, Ž., Glozić, D., Ilić, T., **Litovski, V.**, *"Capacitive Preassure Sensor For Quasi-Static Conditions Followed By A/D Conversion"*, 20th International Conf. on Microelectronics MIEL '95, Vol. 2, Niš, 12.-14. Sep., 1995, pp. 601-604.
35. Panić, V., Milovanović, D., Petković, P., **Litovski, V.**, *"Fault Location In Passive Analog RC Circuits By Measuring Impulse Response"*, 20th International Conf. on Microelectronics MIEL '95, Vol. 2, Niš, 12-14 Sep., 1995, pp. 517-520.
36. Damnjanović, M., Dimić, Ž., **Litovski, V.**, Glozić, D., *"Hardware Description Language For Alecsis Simulator"*, 20th Int. Conf. on Microelectronics, MIEL '95, Vol. 2, Niš, 12-14 Sep., 1995, pp. 525-528.
37. Petković, P., Marković, V., **Litovski, V.**, *"Application Of A Symbolic Simulator In The Education Process"*, 8th Int. Symp. on Theoretical Electronic Engineering, ISTET '95, Thessaloniky, 22-23 Sep., 1995, pp. 529-532.
38. Mrčarica, Ž., Glozić, D., **Litovski, V.**, Detter, H., *"Simulation Of Microsystems Using A Behavioural Hybrid Simulator Alecsis"*, First Int. Conf. on Microsystems and Microstructures, MICROSIM'95, Southampton, 26-28 Sep., 1995, pp. 129-136. Preštampano u celosti u: Adey, R.A., Lahrmann, A., Lemboe Ilmann, C., editors, "Simulation and Design of Microsystems and Microstructures" , Computational Mechanics Publication, Southampton, GB, 1995. Takođe odštampano u celosti u: Transactions on the Built Environment, Vol 12, © 1995 WIT Press, www.witpress.com, ISSN 1743-3509.
39. Milenković, S., Obradović, Z., **Litovski, V.**, *"Annealing Based Dynamyc Learning In Second-Order Neural Networks"*, Int. Conf. on Neural Networks ICNN '96, Washington, D.C., 3.-6. June, 1996, pp. 458-463.
40. Marković, V., Petković, P., **Litovski, V.**, *"Symbolic Approach To The Microwave Circuit Design"*, XI International Microwave Conference MICON '96, Warsaw, 27-30 May, 1996.
41. Ranđelović, Z., **Litovski, V.**, Radović, O., *"Ekspertni sistemi za povezivanje u kanalu"*, Prvi međunarodni Simp.: Industrijsko inženjerstvo '96, Beograd, 1996, pp. 522-524.

42. **Litovski, V.**, Zwolinski, M., Litovski, I., *"Large-Change-Sensitivity Computation In Linear Electronic Circuits"*, Proceedins of 18th International Spring Seminar on Semiconductor and Hybrid Technologies, Sozopol, 1996, pp. 268-274.
43. Milovanović, D., **Litovski, V.**, *"Modeling Procedures And Fault Models Of BiCMOS Logic Circuits"*, Proceedings of 18th International Spring Seminar on Semiconductor and Hybrid Technologies, Vol. 1, Sozopol, 1996, pp. 285-293.
44. Rađenović-Mrčarica, J., Mrčarica, Ž., Detter, H., Brenner, W., **Litovski, V.**, *"Neural Network Visual Recognition Applied To Microelectromechanical Parts Assembly"*, Int. Conf. on Engineering Applications of Neural Networks, EANN '96, Kingston upon Thames, 1996, pp. 325-328.
45. Mrčarica, Ž., Detter, H., Glozić, D., **Litovski, V.**, *"Describing Space-Continous Models Of Microelectromechanical Devices For Behavioural Simulation"*, European Design Automation Conference, EURO-DAC '96 with EURO-VHDL '96, Geneva, 16-20 Sep., 1996, pp. 316-321.
46. Mrčarica, Ž., **Litovski, V.**, Delić, N., Detter, H., *"Modelling Of Micromechanical Devices Using Hardware Description Language"*, 5th Int. Conf. and Exhibition on Micro, Electro, Opto, Mechanical Systems and Components, Microsystem Technologies '96, Potsdam, 17-19 September, 1996, pp. 293-298.
47. Milenković, S., **Litovski, V.**, Obradovic, Z., *"Nondeterminism In Artificial Neural Networks"*, International Memorial Conference D. S. Mitrinovic, Niš, 20-22 Jun, 1996.
48. Keroe, N., Janković, S., Fallman, W., **Litovski, V.**, *"A High Speed Serial Bus Controller ASIC"*, 21st Int. Conf. on Microelectronics, MIEL '97, Vol. 2, Niš, Sep., 1997, pp. 737-740.
49. Janković, S., Maksimović, D., Petković, P., **Litovski, V.**, *"Testable Design Of Digital ASIC With Embedded Analog Multiplexers"*, 21st Int. Conf. on Microelectronics, MIEL '97, Vol. 2, Niš, Sep., 1997, pp. 779-782.
50. Mrčarica, Ž., **Litovski, V.**, Jakovljević, M., Detter, H., *"Hierarchical Modelling Of Microsystems In An Object-Oriented HDL"*, 21st Int. Con. on Microelectronics, MIEL '97, Vol. 2, Niš, Sep., 1997, pp. 475-478.
51. Dimić, Ž., Damnjanović, M., **Litovski, V.**, *"VHDL - Alec++ Cosimulation"*, 21st Int. Conf. on Microelectronics, MIEL '97, Vol. 2, Niš, Sep., 1997, pp. 725-728.
52. Mrčarica, Ž., **Litovski, V.**, Živković, V., *"Delay Time And Crosstalk Simulation In CMOS Integrated Circuits"*, 3rd Int. Conf. on Telecommunications in Modern Satellite, Cable and Broadcasting Services TELSIKS '97, Niš, Oct., 1997, pp. 122-125.
53. Rađenović-Mrčarica, J., Mrčarica, Ž., **Litovski, V.**, Detter, H., *"Application Of Neural Networks In Microsystem Assembly"*, 4th Seminar on Neural Network Applications in Electrical Engineering, NEUREL '97, Beograd, Sep., 1997, pp. 157-160.
54. Milenković, S., Risojević, V., **Litovski, V.**, *"Noise Based Gradient Descent Learning"*, Proc. of 4th Seminar on Neural Networks Appl. in Electrical Engineering, NEUREL '97, Beograd, Sep., 1997, pp. 28-33.
55. Mrčarica, Ž., Ranđelović, Z., Jakovljević, M., **Litovski, V.**, Detter, H., *"Methods For Description Of Microelectromechanical Device Models For System-Level Simulation"*, in Adey,R.A. and Renaud,Ph., ed. "Microsim II, Sec. Inter. Conf. on the Simulation and Design of Microsystems and Microstructures, Proceed.", Lausanne, Sep., 1997, pp. 271-280.
56. Mrčarica, Ž., **Litovski, V.**, Ilić, T., *"Simulation Of The Pressure Sensor Interaction With Its Electronic Environment"*, Micromechanics Europe 1977, Eighth Workshop on Micromachining, Micromechanics and Microsystems, MME '97, Southampton, Kingdom, 31 Aug. - 2 Sep., 1997, pp. 246-249.
57. Aleksić, D., **Litovski, V.**, Milenković, S., *"TCP/IP Protocol Modeling And Simulation Using Alecsis 2.3"*, 3rd Int. Conf. on Telecommunications in Modern Satellite, Cable and Broadcasting Services TELSIKS '97, Niš, Oct., 1997, pp. 564-567.

58. Dokić, B., **Litovski, V.**, Panić, V., *"Novel BiCMOS Driver With Positive Feedback"*, 3rd Int. Conf. on Telecommunications in Modern Satellite, Cable and Broadcasting Services TELSIKS '97, Niš, Yugoslavia, 8-10 Oct., 1997, 126-129.
59. Jakovljević, M., Mrčarica, Ž., Fotiu, P., Detter, H., **Litovski, V.**, "*Implementation Of Finite Elements Using An A-HDL Environment*", Numerische Simulation in Feinwerk-/Mikrotechnik und Elektronik, Munchen, Germany, 4-5 Mart, 1998.
60. Damnjanović, M., **Litovski, V.**, Nikolić, D., Vučković, M., "*CMOS Standard Cell Library Design For Alliance Environment*", Electrical Engineering and Electronics '98, Gabrovo, Dec., 1998, pp. 136-141.
61. Milovanović, D., **Litovski, V.**, "*Komparativni prikaz metoda testiranja CMOS integrisanih kola*", Drugi Simp. industrijska elektronika, INDEL '98, Banja Luka, Sep., 1998, pp. 56-59.
62. Milovanović, D., **Litovski, V.**, "*Iddq Versus Vddt Testing - A Comparative Study*", Electrical Engineering and Electronics, EE '98, Gabrovo, Dec., 1998, pp. 131-135.
63. Petković, P., **Litovski, V.**, Milovanović, D., Panić, V., "*Symbolic Oriented Function Extraction And Fault Modelling Of Analog And Digital Circuits*", Electrical Enineering and Electronics, EE '98, Gabrovo, Dec., 1998, pp. 119-124.
64. Đorđević, S., Živković, V., **Litovski, V.**, Petković, P., "*Determination Of Boundaries Between Frequency Segments During Segmented Symbolic Simulation*", Electrical Engineering and Electronic, EE '98, Gabrovo, Dec., 1998, pp. 125-130.
65. Keroe, N., Janković, S., Fallmann, W., **Litovski, V.**, "*Automatisierter Entwurfs Eines Seriellen Hochgeschwind- igkeits-Bus-Controller-Asics*", Proceedings of AUSTROCHIP '98, Viena, Austria, 1998, pp. 78-82.
66. Shutinoski, G., Dzhekov, T., **Litovski, V.**, "*Motion Perception Via Two Channels Correlation Mechanism: VLSI Proposal For An Object Tracking System Implementation*", Preprints of the IFAC Workshop on Intelligent Components for Vehicles, ICV '98, Seville, March, 1998, pp. 41-46. Published by Pergamon.
67. Shutinoski, V.G., Dzhekov, T.A. and **Litovski, V.B.,** "*Current Mode VLSI Neuromorphic Cell Proposal for Motion Detection*", 42nd MWSCAS, Las Cruces, New Mexico, Aug. 1999, coll. abstracts p. 189.
68. Shutinoski, V.G., Dimirovski, G.A., and **Litovski, V.B.** "*Current Mode VLSI Neural Network for Motion Perception*", Proc. of the 3rd IEEE Int. Conf. on Intelligent Engineering Systems, INES'99, Star Lesn, Slovakia, November, 1999.
69. Mrčarica, Ž., Risojević, V., Lenczner, M., Jakovljević, M., **Litovski, V.**, "*Integrated Simulator For Mems Using FEM Implementation In AHDL And Frontal Solver For Large Sparse Systems Of Equations*", Design, Test and Microfabrication of MEMS, MOEMS '98, CAD, Design and Test, Paris, 30. Mar. - 1. Apr., 1999, pp. 306-315.
70. Maksimović, D., **Litovski, V.**, "*Inverse Circuit Simulation Method For Topological Delays Estimation With Logic Simulator*", 22nd Int. Conf. on Microelectronics, MIEL '99, Niš, May, 2000, pp. 707-710.
71. Petković, P., Đorđević, S., **Litovski, V.**, "*A New Approach To Symbolic Analysis Of Large Circuits*", 22nd Int. Conf. on Microelectronics, MIEL '99, Niš, Yugoslavia, May, 2000, pp. 687-690.
72. Panić, V., Janković, S., Milovanović, D., **Litovski, V.**, "*Cell Design for Boundary-Scan Implementation* ", 22nd Int. Conf. on Microelectronics, MIEL '99, Niš, Yugoslavia, May, 2000, pp. 719-722.
73. Ilić, T., **Litovski, V.**, "*Computationally Efficient Parametric Yield Estimation Of Linear Electronic Circuits* ", 22nd Int. Conf. on Microelectronics, MIEL '99, Niš, Yugoslavia, May, 2000, pp. 683-686.

74. Jakovljević, M., Mrčarica, Ž., Fotiu, P., Detter, H., **Litovski, V.**, "*Analogue Behavioural Simulator As A Tool For Coupled Electro-Thermal Analysis Of Microsystems*", Proc. of the 22nd Int. Conf. on Microelectronics, MIEL '99, Niš, Yugoslavia, May, 2000, pp. 561-564.
75. Zarković, K., Ilić, T., Savić, M., and **Litovski, V.**, "*ANN application in Modeling of Dynamic Two-Terminal Linear Circuits*", Proceeding of ETAI'2000, September 2000, Ohrid, pp. E-27-E-30.
76. Mrčarica, Ž., Maksimović, D., Tasić, A., and **Litovski, V.**, "*Some features of analogue and Mixed-Signal HDL AleC++*", Proceedings of SSSS2000, Niš, September 2000, pp. 37-42.
77. Jakovljević, M., Fotiu, P., Mrčarica, Ž., **Litovski, V.,** and Detter, H., "*Electro-thermal simulation of microsystems with mixed abstraction modelling*", Proceedings of SSSS2000, Niš. Sept. 2000, pp. 13-22.
78. Ilić, T., Zarković, K., **Litovski, V**., and Damper, R., "*ANN Application in Modelling of Dynamic Linear Circuits*", Proceedings of SSSS2000, Niš. Sept. 2000, pp. 43-47.
79. Petković, P., Bushehri, E., Milenković, S., and **Litovski, V.**, "*A high level simulation for ΣΔ Modulator Design*", Proceedings of SSSS2000, Niš. Sept., 2000, pp. 53-56.
80. Shutinoski, G.V. Dzhekov, T.A. **Litovski, V.B.** , "*Current mode elementary motion perception neural cell*", Proceedings of the IEEE International Symposium on Circuits and Systems, ISCAS 2000, Volume: 3, On page(s): 157-160 vol.3, Meeting Date: 05/28/2000 - 05/31/2000, Location: Geneva, Switzerland, ISBN: 0-7803-5482-6.
81. **Litovski, V.,** Savić, M., "*Circuit-theoretical approach to feedback system analysis*", Electronics ET2001, Sofia, Sept., 2001, pp. 47-52.
82. Stefanović, D., Sokolović, M., Petković, P., and **Litovski, V**., "*T-Spice-Alecsis Co-simulation*", Proceedings of MIEL'02, Niš, 2002, pp. 625-628.
83. Andrejević, M., Milovanović, D., Petković, P., **Litovski,** V., "*Extraction of Frequency Characteristics of Switched-Capacitor Circuits Using Time-Domain Analysis*", Proceedings of MIEL'02, Niš, 2002 pp. 635-638.
84. Maksimović, D., **Litovski, V.,** "*Timing Simulation With VHDL Simulators*", Proceedings of MIEL'02, Niš, 2002, pp. 655-658.
85. Andrejević, M., **Litovski, V.**, "*ANN Aplication In Modelling of Chua's Circuit*", Proc. of Neurel 2002, Belgrade, September 2002, pp. 119-122.
86. Andrejević, M., **Litovski, V.,** "*Non-Linear Dynamic Network Modelling Using Neural Networks*", Int. Congress on Computional and Applied Mathematics, Leuven, Belgium, 22.July-26.July, 2002, pp. 16.
87. **Litovski, V.,** Damnjanović, M., Andjelković,B., "*ALECSIS/VHDL–AMS Mixed Language Simulation*", Proc. of The 11th Int. Scientific and Appl. Sci. Conf. Electronic ET2002, Sozopol, Sep., 2002. Vol. 1, pp. 25-30
88. Stefanović D., Pastre, M., Kayal, M., and **Litovski, V.,** "*Chart Oriented CAD Tool for CMOS Transistor Sizing*", Proc. of the 11th Int. Scientific and Appl. Sci. Conf. of Electronics ET2002, Sep., 2002, Sozopol, Vol. 2, pp. 95-100
89. Savić, M., **Litovski, V**., "*Frequency Domain Electronic Circuit Analysis in an Object Oriented Environment*", Proc. of the 11th Int. Scientific and Appl. Sci. Conf. of Electronics ET2002, Sep., 2002, Sozopol, 2002. Vol. 2, pp. 65-70
90. Stefanović, D., Kayal, M., Paste, M., **Litovski, V. B.,** "*Procedural Analog Design (PAD) Tool*", IEEE ISQED 2003, 4th Int. Symp. on Quality Electronic Design, 24-26 March 2003, San Jose, California, pp. 313-318
91. Milojković, J., Jovanović, S., **Litovski, V.,** "*Information Infrastructure for Sustainable Product Design System*", Proceedings Colloquium e-ecological Manufacturing, 2003, Berlin, pp. 75-77

92. **Litovski V.**, Andrejević M., Damper. R., *"Modeling the d/a interface for mixed-mode behavioral simulation"*, EUROCON 2003, Ljubljana, Sept. 2003, pp. A130-A133.
93. Andrejević, M., and **Litovski, V.,** *"ANN application in electronic diagnosis - Preliminary results"*, Proceedings of MIEL'04, Niš, 2004, Vol. 2, pp. 597-600.
94. **Litovski, V.,** Andrejević, M., and Zwolinski, M., "*ANN based modeling, testing, and diagnosis of MEMS*", Proc. of the 7th Seminar on Neural network Applications in Electronic engineering, NEUREL 2004, Sept. 2004, Belgrade, pp. 183-188.
95. Milenković, S., and **Litovski, V.,** "*Passive image rejection filters optimized for telecommunication applications*", Small Systems Simulation Symposium, SSSS'05, Niš, 2005, pp. 39-49.
96. Litovski, V., Andrejević, M., and Zwolinski, M., "*Acceleration of MEMS fault simulation using ANNs*", Small Systems Simulation Symposium, SSSS'05, Niš, 2005, pp. 50-54.
97. Savić, M., and **Litovski, V.,** "*Bandgap Voltage reference in CMOS*", Small Systems Simulation Symposium, SSSS'05, Niš, 2005, pp. 55-58.
98. Dimitrijević, M., and **Litovski, V.,** "*Implementation of the component characteristic curve tracer using PC-based acquisistion card*", Small Systems Simulation Symposium, SSSS'05, Niš, 2005, pp. 63-66.
99. **Litovski V.,** Andrejevic M., Zwolinski M.,"Behavioural Modelling, Simulation, Test and Diagnosis of MEMS using ANNs", 2005 IEEE International Symposium on Circuits and Systems, Kobe, Japan, 2005, pp. 5182-5185.
100. Dimitrijević,M., and **Litovski, V**.,"*Computer Integrated Analogue Electronics Laboratory for Undergraduate Teaching*", Proceedings of the Remote Engineering and virtual instrumentation Symposium, REV2005, Brasov, Romania, June 30- July 01, 2005, www.online-lab.net-rev.
101. Savić, M., Mrčarica, Ž., and **Litovski, V.,**: "*Computationally Efficient Simulation of Nonlinear Communication Circuits with Switches*", 7th WSEAS Int. Conf. on Mathematical Methods and Computational Techniqeues in Electrical Engineering, WSEAS MMACTEE'05, Sofia, Bulgaria, October 2005, pp. 69-74.
102. Sokolović, M., and **Litovski, V.,** "*Using VHDL Simulator to Estimate Logic Path Delays in Combinational and Embedded Sequential Circuits*", IEEE Region 8 EUROCON 2005 conference, Belgrade, November 21-24, 2005, pp. 1683-1686.
103. Dimitrijević,M., and **Litovski, V**., "*Specific analog electronic circuits analysis using PC-based acquisition card*", IEEE Region 8 EUROCON 2005 conference, Belgrade, November 21-24, 2005, pp. 910-913.
104. Andjelković,M., **Litovski, V**., and Zerbe, V., "*New aspects in HDL's performance evaluation*", IEEE Region 8 EUROCON 2005 conference, Belgrade, November 21-24, 2005, pp. 499-502.
105. **Litovski, V.,** Milojković, J., and Jovanović, S., *"A concept of education in sustainable electronic design"*, Proc. of the Int. Symposium: Waste Management and the Environment III, Malta, June 2006, pp. 415-424. Published by WIT Press, V. Popov, Editor.
106. Andjelković,M., **Litovski, V**., and Zerbe, V., *"A Mission Level Design Language Based on Alec++"*, Proc. Of the 25th Int. Conf. On Microelectronics (MIEL 2006), Belgrade, Serbia and Montenegro, 14-17 May, 2006, pp. 659-662.
107. **Andrejević, M.,** Litovski, V., and Zwolinski, M., *"Fault Diagnosis in Digital Part of Mixed-Mode Circuits"*, Proc. Of the 25th Int. Conf. On Microelectronics (MIEL 2006), Belgrade, Serbia and Montenegro, 14-17 May, 2006, pp. 437-440.
108. Dimitrijević, M., and **Litovski, V.,** «*Power factor and distortion measuring for small loads using USB acquisition module*», Int. Symp. on Remote Engineering and Virtual Instrumentation, REV 2006, Maribor, Slovenia, June 2006. Paper No. SID5.1/2.

109. Andrejević, M., and **Litovski, V.,** «*Fault diagnosis in digital part of sigma-delta converter*», Proceedings of the 8th Seminar on Neural network application in electrical engineering, NEUREL ' 2006, pp. 177-180.
110. **Litovski, V.,** Andrejević, M., and, Nikolić, M., «*Chaos based analog-to-digital conversion of small signals*», Proceedings of the 8th Seminar on Neural network application in electrical engineering, NEUREL ' 2006, pp. 173-176.
111. Anđelković B., Dimitrijević, M., and **Litovski, V.,** „*Using grid computing in parallel electronic circuit simulation*", Electronics' 2007, 19 – 21 September, Sozopol, Bulgaria, book 4, pp. 109-114.
112. Dimitrijević M., and **Litovski, V.,** „*Implementation of compact switching power supply with high power factor*", Electronics' 2007, 19 – 21 September, Sozopol, Bulgaria, pp. 129-132.
113. **Litovski, V.,** and Andrejević, M., „*Nonlinear modelling in biomedical applications using ANNs*", Proc. Of the International Conference on Biomedical Electronics and Devices, Biodevices 2008,28. - 31. january 2008., Funchal, Madeira, Portugal, Vol. 1, pp.115-116.
114. Andrejević, M., and **Litovski, V.,** „*Hierarchical Approach To Diagnosis Using ANNs* ", Proc. 26th International Conference On Microelectronics (Miel 2008), Niš, Serbia , 11-14 May, 2008, pp. 395-398.
115. Sokolović, M., Petković, P., and **Litovski, V.,** "*Design for Testability for SoC Based on IDDQ Scanning*", Proc. 26th International Conference On Microelectronics (Miel 2008), Niš, Serbia , 11-14 May, 2008, pp. 407-410.
116. Milojković, J. and **Litovski, V.,** "Comparison of Some ANN Based Forecasting Methods Implemented on Short Time Series", 9th Symposium on Neural Network Applications in Electrical Engineering, NEUREL-2008, Belgrade, 2008, pp. 179-179.
117. Milojković, J., and Litovski, V.B., "Prediction in Electronics based on limited information", Proceedings of the 8th WSEAS Int. Conf. on Electronics, Hardware, wireless and optical communications, EHAC'09, Cambridge, UK, Februarz 2009, pp. 33-38.
118. Petković, P., Trajanov, D., Grnarov, A., and Litovski, V., "*System On Chip Design: New Harmonized Master Studies Curriculum in Macedonia And Serbia*", Ninth National Conference with International Participation, ETAI 2009, Ohrid, Macedonia, September 2009, Proc. on disc, Paper No. IE1-2.
119. Milojković, J. and Litovski, V.B., „Short-term forecasting of the electricity load at suburban level", Ninth National Conference with International Participation, ETAI 2009, Ohrid, Macedonia, September 2009, Proc. on disc, paper No. A2-1.
120. Litovski, V. B., "*Twenty years of ANN research and application in LEDA*", Small systems simulation symposium, Niš, February 2010, ISBN 987-86-6125-006-4, pp. 33-41.
121. Milojković, J., and Litovski, V., "*Multistep forecasting in electronics based on reduced information*", Small systems simulation symposium, Niš, February 2010, ISBN 987-86-6125-006-4, pp. 42-48.
122. Anđelković, B., Dimitrijević, M., Andrejević Stošović, M., Litovski, V., "*Parallelizing Electronic Circuit Simulation on Multicore Computer Cluster*", Small systems simulation symposium, Niš, February 2010, ISBN 987-86-6125-006-4, pp. 71-74.
123. Dimitrijević, M., and Litovski, V., "*Computer Based Power Factor and Distortion Measuring for Small Loads*", Small systems simulation symposium, Niš, February 2010, ISBN 987-86-6125-006-4, pp. 81-85.

Radovi na domaćim Konferencijama

1. Lazović, S., **Litovski, V.**, *"Ka problemu aproksimacije konstantnog grupnog kašnjenja"*, XIV Konf. ETAN-a, Sarajevo, Juni, 1970, pp. 25-35.
2. Lazović, S., **Litovski, V.**, *"Jedna nova metoda sinteze prenosne funkcije za kompresiju impulsa"*, XVI Konf. ETAN-a, Velenje, Juni, 1971, pp. 373-381.
3. Lazović, S., **Litovski, V.**, Radmanović,M., *"Automatsko projektovanje niskopropusnih lestvičastih filtara sa zadatim karakteristikama"*, XVIII Konf. ETAN-a, Ulcinj, Juni, 1974 , pp. 290-297.
4. Radmanović, M., **Litovski, V.**, Lazović,S., *"Algoritam za automatsku sintezu prelaznih Thomson-Butterworth-ovih filtara"*, XVIII Konf. ETAN-a, Ulcinj, 1974.
5. **Litovski, V.**, Lazović, S., *"Automatsko projektovanje generalnog fitra"*, XIX Konf. ETAN-a, Ohrid, Juni, 1975, pp. 129-138.
6. **Litovski, V.**, *"Gaussov filtar sa modifikovanom karakterističnom funcijom"*, XX Konf. ETAN-a, Opatija, 1976.
7. **Litovski, V.**, Stojanović, V., Lazović, S., Radmanović, M., *"Realizacija uskopojasnog aktivnog filtra sa specijalnim zahtevima u prelaznoj zoni"*, YUTEL 76, Simp. o telekomunikacijama, Ljubljana, 1976, pp. C/VII--1-C/VII-7.
8. Lazović, S., **Litovski, V.**, *"O jednoj novoj klasi selektivnih filtara sa linearnom faznom karakteristikom"*, XXI Konf. ETAN-a, Banja Luka, Jun, 1977, pp. I.243-I.249.
9. **Litovski, V.**, Milovanović, D., *"Selektivni polinomski filtri sa linearnom faznom karakteristikom"*, Zbornik radova XXI Konf. ETAN-a, Banja Luka, Juni, 1977, pp. I.251-I.257.
10. **Litovski, V.**, Milovanović, D., *"Sinteza neminimalno-faznih filtarskih funkcija s suboptimalnom karakteristikom grupnog kašnjenja"*, Zbornik radova XXII Konf. ETAN-a, Zadar, Juni, 1978, pp. I.289-I.296.
11. **Litovski, V.**, Petković, P., *"Jedan metod simulacije elektronskih kola sa MOS tranzistorima"*, MIEL 79, Simp. o mikroelektronici, Beograd, 1979, pp. 77-83.
12. Milovanović, D., **Litovski, V.**, *"Jedan metod sinteze prenosnih funkcija za prenos podataka"*, Zbornik radova XXIII Konf. ETAN-a, Maribor, Juni, 1979, pp. I.177-I.182.
13. **Litovski, V.**, Lazović, S., *"Jedna nova metoda sinteze filtara sa linearno opadajućim grupnim kašnjenjem"*, XXIII Konf. ETAN-a, Maribor, Juni, 1979, pp. I.169-I.176.
14. Radović, R., **Litovski, V.**, *"Neka iskustva u modeliranju i simulaciji kardiovaskularnog sistema"*, Simp. "Biomedicinska elektronika", Skoplje, april, 1980, pp. 60-85.
15. **Litovski, V.**, Simonović, V., *"Simulacija prelaznih režima u kolima sa MOS tranzistorima"*, MIEL 80, Simp. o mikroelektronici, Niška Banja, april, 1980, pp. 215-221.
16. **Litovski, V.**, Petković, P., *"Razvoj softvera za simulaciju elektronskih kola sa MOS tranzistorima"*, II Znanstveni skup: Numeričke metode u tehnici, Stubičke Toplice, novembar, 1980, pp. 145-155.
17. Milovanović, D., **Litovski, V.**, "*Jedan metod sinteze prenosnih funkcija filtara za prenos govora i impulsa*", Zbornik radova XXV Jug. Konf. ETAN-a, Mostar, juni, 1981, pp. i.165-i.171.
18. **Litovski, V.**, Petković, P., "*Algoritam za kontrolu koraka pri numeričkoj integraciji jednačina elektronskih kola*", III znanstveni skup "Numeričke metode u tehnici", Stubičke toplice, Nov., 1981, pp. 599-607.
19. **Litovski, V.**, Đorđević, S., Stojanović, Z., Petković, P., Pantić, S., "*MOST-program za simulaciju prelaznih režima u kolima sa MOS tranzistorima*", Zbornik radova XXVI Jug. Konf. ETAN-a, Subotica, jun, 1982, pp. i.19-i.26.
20. Damnjanović, M., Milićević, M., **Litovski, V.**, "*Projektovanje integrisanih kola: problem layout-a*", Zbornik radova X Jug. savet. o mikroelektronici, MIEL 82, Banja Luka, april, 1982, pp. 85-116.

21. **Litovski, V.**, Ristić, S., Petković, P., *"Simulacija temperaturske zavisnosti električnih karakteristika kola sa MOS tranzistorima"*, Zbornik radova XXVII Jug. Konf. ETAN-a, Struga, Jun, 1983, pp. II.43-II.48.
22. Damnjanović, M., **Litovski, V.**, *"Povezivanje ćelija u integrisanom kolu"*, Zbornik radova XI Jug. savet. o mikroelektronici MIEL 83, Zagreb, april, 1983, pp. 47-54.
23. Milićević, M., **Litovski, V.**, *"Algoritam za razbijanje ortogonalnih likova na pravougaonike"*, Zbornik radova XII Jug. savet. o mikroelektronici, MIEL 84, Niš, maj, 1984, pp. 203-208.
24. **Litovski, V.**, Petković, P., *"Električna karakterizacija ćelija u gejtovskoj matrici GEM 21"*, Zbornik radova XII Jug. savet. o mikroelektronici, MIEL 84, Niš, 7-9. maj, 1984, pp. 209-214.
25. Milovanović, D., **Litovski, V.**, *"Upotreba modifikovane metode čvorova za simulaciju SC kola u frekventnom i vremenskom domenu"*, Zbornik radova XXVIII Jug. Konf. ETAN-a, Split, Jun, 1984, pp. V.109-V.116.
26. Stojanović, Z., **Litovski, V.**, *"Modeli ćelija u logičkom simulatoru LOST"*, Zbornik radova XIII Jug. savet. o mikroelektronici MIEL 85, Ljubljana, maj, 1985, pp. 115-122.
27. Pantić, S., **Litovski, V.**, *"Programska realizacija električnog modela MOS tranzistora u oblasti zakočenja"*, Zbornik radova XIII Jug. sav. o mikroelektronici, MIEL 85, Ljubljana, 1985, pp. 283-290.
28. Stojanović, Z., **Litovski, V.**, *"Logička simulacija upotrebom programa LOST"*, Zbornik radova XXIX Jug. Konf. ETAN-a, sveska 2, *Proglašen za najbolji rad u Komisiji za elektroniku i dodeljena nagrada Branko Raković*, Niš, Jun, 1985, pp. 21-28.
29. Damnjanović, M., **Litovski, V.**, *"Jedno rešenje problema povezivanja u kanalu gejtovske matrice GEM 21"*, Zbornik radova XXIX Jug. Konf. ETAN-a, Niš, Jun, 1985, pp. VIII.211-VIII.218.
30. **Litovski, V.**, Petković, P., *"Ka simulaciji elektronskih kola visokog stepena integracije"*, Zbornik radova II Tematske Konf. za ETAI, ETAI '85, Ohrid, oktobar, 1985, pp. 1-8.
31. **Litovski, V.**, *"O stanju opreme i programske podrške za projektovanje mikroelektronskih kola u SR Srbiji"*, Zbornik radova savet. "Stanje programske i aparaturne opreme za projektovanje elektronskih kola", Maribor, novembar, 1985, pp. 59-62.
32. Stojanović, Z., **Litovski, V.**, *"Modeliranje kašnjenja logičkih operatora pri različitim nivoima logičke simulacije"*, Zbornik radova XXX Jug. Konf. ETAN-a, Herceg Novi, jun, 1986, pp. II.123-II.130.
33. Petković, P., **Litovski, V.**, *"Makroanaliza vrlo složenih CMOS kola"*, Zbornik radova VIII Medjunarodnog simpozija "Kompjuter na sveučilištu", Cavtat, maj, 1986, pp. 2.15-1 - 2.15-8.
34. Kocić, A., **Litovski, V.**, *"Korišćenje programa za analizu linearnih kola u nastavi"*, Zbornik radova VIII Medjunarodnog simpozija "Kompjutor na sveučilištu", Cavtat, maj, 1986, pp. 1A.02-1 - 1A.02-5.
35. Đorđević, S., **Litovski, V.**, *"Modeliranje i programska realizacija saturacione oblasti bipolarnog tranzistora"*, Zbornik radova XV Jug. savet. o mikroelektronici, MIEL-87, Banja Luka, Maj, 1987, pp. 269-276.
36. **Litovski, V.**, Petković, P., *"Razvoj makromodela CMOS logičkih operatora u vremenskom domenu"*, Zbornik radova XV Jug. sav. o mikroelektronici MIEL-87, Banja Luka, Maj, 1987, pp. 55-62.
37. Đorđević, S., **Litovski, V.**, *"Modeliranje i programska realizacija modela bipolarnog tranzistora"*, Zbornik radova XXXI Jug. Konf. ETAN-a, ETAN 87, Bled, Juni, 1987, pp. x.19-x.26.

38. Damnjanović, M., **Litovski, V.**, *"Uticaj redosleda trasiranja veza na konačnu topologiju kanala u gejtovskoj matrici GEM 21"*, Zbornik radova XXXI Jug. konf. ETAN-a, ETAN '87, Bled, Juni, 1987, pp. x.35-x.42.
39. **Litovski, V.**, Milovanović, D., Stojanović, Z., *"Mogućnosti programa ulaznog jezika lostin za logički simulator LOST"*, Zbornik radova XV Jug. sav. o mikroelektronici MIEL 87, Banja Luka, Maj, 1987, pp. 507-512.
40. Milićević, M., **Litovski, V.**, Vacić, Z., Kocić, A., *"Koncepcija razvoja softvera za projektovanje integrisanih kola tipa GEM"*, Zbornik radova Simp.a "Projektiranje i proizvodnja podržani računalom (pppr)", Zagreb, Oktobar, 1987, pp. 435-440.
41. **Litovski, V.**, Đorđević, S., Petković, P., *"Analiza bipolarnih i MOS kola programom MOST"*, Zbornik radova XVI Jug. savet. o mikroelektronici, MIEL 88, Tom I, Zagreb, Maj, 1988, pp. 303-310.
42. Stojanović, Z., **Litovski, V.**, *"Algoritam kontrole toka vremena u logičkom simulatoru LOST"*, Zbornik radova XVI Jug. savet. o mikroelektronici, MIEL 88, Tom I, Zagreb, Maj, 1988, pp. 271-278.
43. Milenković, S., **Litovski, V.**, *"Pregled algoritama za inicijalni razmeštaj ćelija u integrisanom kolu tipa GEM"*, Zbornik radova XXXII Jug. konf. ETAN-a, Sarajevo, 6-10 Jun, 1988, pp. x.123-x.130.
44. Radenković, Z., Janković, T., Janićijević, I., **Litovski, V.**, *"SED: An Interactive Symbolic Gate-Array Editor"*, XVII Yugoslav conf. on microelectronics, MIEL 89, Niš, 9-11 Maj, 1989, pp. 577-582.
45. Petković, P., **Litovski, V.**, *"Modeliranje izlazne otpornosti CMOS logičkih operatora"*, III tematski Simp. za ETAI, ETAI '89, Ohrid, Sept., 1989, pp. 29-38.
46. Stojanović, A., **Litovski, V.**, *"Automatizacija projektovanja niskofrekventnih SC-filtara"*, III tematski Simp. za ETAI, ETAI '89, Ohrid, Sept., 1989, pp. 92-100.
47. Milovanović, D., Nikolić, J., Damnjanović, M., **Litovski, V.**, *"Konverzija logičke u topološku šemu integrisanog kola pomoću programa COSILA"*, III tematski simp. za ETAI, ETAI '89, Ohrid, Sept., 1989, pp. 150-159.
48. Janković, T., Radenković, Z., **Litovski, V.**, *"Integrisani softverski paket za projektovanje gejtovske matrice (ISPGM)"*, III tematski simp. za ETAI, ETAI 89, Ohrid, Sept., 1989, pp. 62-71.
49. Milovanović, D., **Litovski, V.**, Petković, P., *"Model Generation Of Faulty Logic Circuits"*, XVII Yugoslav conference on microelectronics, MIEL 89, Niš, Maj, 1989, pp. 545-550.
50. Damnjanović, M., **Litovski, V.**, Mrčarica, Ž., *"Programski paket za generisanje veza na integrisanom kolu"*, III tematski Simp. za ETAI, ETAI '89, Ohrid, Septembar, 1989, pp. 72-81.
51. Milovanović, D., Jevtić, M., **Litovski, V.**, *"Modeliranje defekata u sekvencijalnim kolima"*, Zbornik radova XXXIV Jug. Konf. ETAN-a, ETAN '90, Zagreb, Juni, 1990, pp. 137-144.
52. Petković, P., **Litovski, V.**, Glozić, D., *"Novi model izlazne otpornosti CMOS logičkih operatora"*, Zbornik radova XXXIV Jug. Konf. ETAN-a, ETAN '90, Zagreb, 4-8 Juni, 1990, pp. 27-34.
53. Milovanović, D., **Litovski, V.**, *"Modifikovani metod konkurentne simulacije defekata"*, Zbornik radova XXXV Jug. Konf. ETAN-a, Ohrid, Jun, 1991, pp. 195-202.
54. **Litovski, V.**, Rađenović, J., Mrčarica, Ž., Milenković, S., Zografski, Z., *"Modeliranje MOS tranzistora neuronskom mrežom"*, Zbornik radova XXXVI Konf. ETAN-a, Vol. II, Kopaonik, 28.9-1.10, 1992, pp. 19-25.

55. Maksimović, D., Mrčarica, Ž., Glozić, D., Petković, P., **Litovski, V.**, *"Arhitektura programa i strukture podataka u hibridnom simulatoru"*, Zbornik radova XXXVI Konf. ETAN-a, Vol. II, Kopaonik, 28.9-1.10, 1992, pp. 27-34.
56. **Litovski, V.**, Ranđelović, Z., *"Primena greedy strategije pri povezivanju u switchbox-u"*, Zbornik radova XXXVI Konf. ETAN-a, Vol. II, Kopaonik, 28.9-1.10, 1992, pp. 3-9.
57. Milovanović, D., **Litovski, V.**, Jevtić, M., *"Generisanje modela MSD flip-flopa sa defektom"*, Zbornik radova Prve Srpske Konf. o Mikroelektronici i Optoelektronici, MIOPEL '92, Vol. I, Beograd, Oktobar, 1992, pp. 1.3.2.1-1.3.2.8.
58. Ranđelović, Z., **Litovski, V.**, Damnjanović, M., *"Efikasni kanalni algoritam - ECTAN"*, Zbornik radova Prve Srpske Konf. za Mikroelektroniku i Optoelektroniku, MIOPEL '92, Vol. I, Beograd, Okt., 1992, pp. 1.3.1.1-1.3.1.8.
59. Mrčarica, Ž., **Litovski, V.**, *"Some Considerations Of Short-Channel MOS Model Selection For A Circuit Simulation Program"*, Zbornik radova Prve Srpske Konf. o Mikroelektronici i Optoelektronici, MIOPEL '92, Vol. I, Beograd, Okt., 1992, pp. 1.3.4.1-1.3.4.6.
60. Bajić, N., Milovanović, D., **Litovski, V.**, Dokić, B., *"Generisanje modela defekata CMOS trostatičkog invertora"*, Zbornik radova Prve Srpske Konf. o Mikroelektronici i Optoelektronici, MIOPEL '92, Vol. I, Beograd, Oktobar, 1992, pp. 1.3.3.1-1.3.3.10.
61. Maksimović, D., Milentijević, I., **Litovski, V.**, *"Projektovanje i logička simulacija cifarsko-serijskog množača"*, Zbornik radova XXXVII Konf. ETAN-a, Beograd, Sept., 1993.
62. Glozić, D., Rađenović, J., **Litovski, V.**, *"Implementacija MOS tranzistora modeliranog neuronskom mrežom u hibridnom simulatoru Alecsis"*, Zbornik radova XXXVII Konf. ETAN-a, Beograd, Sept., 1993.
63. Ranđelović, Z., **Litovski, V.**, *"Brzi algoritam za globalno trasiranje"*, Zbornik radova XXXVII Konf. ETAN-a, Vol. II, Beograd, 20-23 Sept., 1993, pp. 195-200.
64. Petković, P., Marković, M., Stevanović, R., Milovanović, D., **Litovski, V.**, *"Primena simboličke analize u projektovanju VF kola"*, TELSIKS '93, Niš, Okt., 1993, pp. VI-15-22.
65. Glozić, D., **Litovski, V.**, *"Primena paketa ASCOTA3 ADIL za projektovanje telekomunikacionih analognih integrisanih kola"*, TELSIKS '93, Niš, Okt., 1993, pp. VI-7-14.
66. Stevanović, R., Petković, P., Milovanović, D., Marković, V., **Litovski, V.**, *"Simbolički pristup analizi vf pojačavača"*, TELSIKS '93, Niš, Okt., 1993, pp. VI-23-30.
67. Maksimović, D., Milentijević, I., **Litovski, V.**, *"Projektovanje i logička simulacija cifarsko-serijskog množača"*, Zbornik radova XXXVII Konf. ETAN-a, Beograd, Sept., 1993, Vol. VIII, pp. 221-226.
68. Zarković, K., **Litovski, V.**, Stojilković, S., *"Ubrzanje učenja veštačkih neuronskih mreža statističkim metodama"*, Zbornik radova XXXVIII Jug. konf. ETRAN-a, Vol. III, Niš, Jun, 1994, pp. 205-206.
69. Maksimović, D., Glozić, D., **Litovski, V.**, *"Trendovi razvoja elektronskih simulatora - Alecsis2.1 hibridni simulator"*, X Scientific Conference Man and Working Environment: Preventive Engineering and Information Technologies, Niš, Dec., 1994, pp. 25-1-25-8.
70. Milenković, S., Obradović, Z., **Litovski, V.**, *"Dinamičko učenje neuronskih mreža drugog reda zasnovano na simuliranom očvršćavanju"*, 3rd Seminar on Neural Netvork Applications in Electrotechnics NEUREL-95, Belgrade, Yugoslavia, Sep., 1995.
71. Aleksić, D., **Litovski, V.**, Milenković, S., *"Modeliranje i simulacija ethernet bridgea logičkim simulatorom Alecsis 2.1"*, TELSIKS '95, Niš, Okt., 1995, pp. 400-403.
72. Petković, P., Marković, V., **Litovski, V.**, *"Simbolička analiza mikrotalasnih kola u funkciji talasnih parametara"*, TELSIKS '95, Niš, Oct., 1995, pp. 400-403.
73. Ranđelović, Z., **Litovski, V.**, Radović, O., Cvetković, S., *"Simultana konstrukcija Štajnerovog stabla veza pri projektovanju topologije VLSI IC"*, YU INFO '96, Brezovica, April, 1996, pp. 244-247.

74. Milenković,S., Stanković,M., **Litovski,V.**, *"Veštačke neuronske mreže u otkrivanju i dijagnozi otkaza dinamičkih sistema"*, Međunarodna Konf. Tehnički sistemi i sredstva zaštite od požara, eksplozija, havarija i provala, Beograd, Nov., 1996.
75. Milenković, S., Milošević, Z., **Litovski, V.**, Zarković, K., *"Računarske mreže u projektovanju pomoću računara"*, Zbornik radova, IV Telekomunikacioni forum TELFOR '97, Beograd, Sept., 1996, pp. 52-55.
76. **Litovski, V.**, *"Uticaj novih tejnologija u elektronici na razvoj velikih sistema"*, Zbornik radova, XIV naučno stručni Simp. o novim tehnologijama u PTT, Beograd, Dec., 1996, pp. 175-184.
77. Aleksić, D., **Litovski, V.**, Milenković, S., *"Modeliranje i primena modela TCP/IP protokola u Alecsis 2.3 simulatoru"*, Zbornik Radova YUINFO '97, Brezovica, Apr., 1997, pp 425-428.
78. **Litovski, V.**, Milovanović, D., *"Hardware Description Languages For Analog And Mixed-Signal Design"*, Prvi simp. industrijska elektronika INDEL '97, Banja Luka, Sep., 1997, pp. 96-100.
79. Milenković, S., Janković, N., Litovski, I., Živković, V., **Litovski, V.**, Milovanović, D., *"Kolo za power-on-reset u standarnoj CMOS tehnologiji"*, Prvi Simp. industrijska elektronika INDEL '97, Banja Luka, Sept., 1997, pp. 118-123.
80. Janković, S., Maksimović, D., Živković, V., Petković, P., **Litovski, V.**, *"Testabilno digitalno integrisano kolo specifične namene sa ugrađenim analognim multiplekserima"*, Prvi Simp. industrijska elektronika INDEL '97, Banja Luka, Sep., 1997, pp. 124-128.
81. Ranđelović, Z., Zarković, K., **Litovski, V.**, *"Računarsko projektovanje štampanih tkanina"*, Simp. Pravci razvoja tekstilne industrije za treći milenijum, Niš, Okt., 1997, pp. 270-279.
82. Zarković, K., Milenković, S., **Litovski, V.**, *"Primena računarskih mreža pri integraciji CAD sistema u tekstilnoj industriji"*, Simp. Pravci razvoja tekstilne industrije za treći milenijum, Niš, Okt., 1997, pp. 263-269.
83. Milenković, S., **Litovski, V.**, Stanković, M., *"Veštačke neuronske mreže u otkrivanju i dijagnozi otkaza dinamičkih sistema"*, Zbornik radova međunarodne Konf.: Tehnički sistemi i sredstva zaštite od požara, eksplozija, havarija i provala, 1997.
84. Zarković, K., Milenković, S., **Litovski, V.,** "*Primena računarskih mreža pri integraciji informacionih sistema u medicini*", XIII Info-teh '98, Zbornik radova, Vrnjačka Banja, Jun, 1998, pp. 156-160.
65. Đorđević, S., **Litovski, V.**, Petković, P., "*Određivanje granice između frekvencijskih segmenata u okviru segmentne simboličke simulacije*", Drugi Simp. industrijska elektronika INDEL '98, Banja Luka, Sep., 1998, pp. 87-92.
86. Petković, P., **Litovski, V.**, Tošić, D., "*Simbolička analiza elektronskih kola, savremeni razvoj i industrijska primena*", Drugi Simp. industrijska elektronika, INDEL '98, Banja Luka, Sep., 1998, pp. 11-16.
87. **Litovski, V.,** Damnjanović, M., and Andjelković, B., "*CAD sistemi zasnovani na VHDL okruženju*", VJ INFO 2001, Beograd 03.04.2001, CK VJ, 2001 (publikacija na CD ROMu)
88. Milojković, J., **Litovski, V.,** "*Ekološki aspekt projektovanja u elektronici*", Zbornik radova XLVI konf. ETRAN-a, ETRAN 2002, Jun 2002, Banja Vrućica, pp. I.66-I.79
89. **Litovski, V.**, Andrejević, M., "*ANN Application In Modelling of A/D Interfaces for Mixed-Mode Behavioral Simulation*", Proc. of the XLVI Conf. of ETRAN, ETRAN 2002, June 2002, Banja Vrućica, pp. I.51-I.54.
90. Milojković, J., **Litovski, V.**, "*Održivo projektovanje u elektronici*", Proc. of the International Conference on Dependability and Quality Management, DQM-2002, Belgrade, June 2002, pp. 348-354.

91. Savić, M., **Litovski, V.**, "*Implementation of a New Object Oriented Frequency Domain Electronic Circuit Simulation System*", Proc. of the IV Symp. Industrial Electronics, INDEL 2002, Banja Luka, Nov. 2002, pp. 166-168.
92. Stefanović D., Kayal M., **Litovski V. B.**, "*An Interactive Knowledge Based Analog Design Approach*", Proc. of the IV Symp. Industrial Electronics, INDEL 2002, Banja Luka, November 2002, pp. 173-176.
93. **Litovski, V.**, i Andrejević, M., "*Modelovanje d/a sprege za hibridnu funkcionalnu simulaciju*", Zbornik radove XLV Konf. ETRAN-a, ETRAN 2003, Jun 2003, Herceg Novi, Vol. 1, pp. 76-79.
94. Nikolić, M., i Litovski, V., "*CMOS implementacija hopfildove neuronske mreže*", Zbornik radova XLV Konf. ETRAN-a, ETRAN 2003, Jun 2003, Herceg Novi, Vol. 1, pp. 132-135.
95. Savić M., **Litovski, V.**, "*Behavioral object-oriented frequency domain electronic simulation*", VI nacionalna Konf. ETAI,Ohrid, 17.-20. septembar 2003., pp. E1-E4.
96. **Litovski, V.**, and Andrejević, M., "*ANN aplication in electronic circuits diagnosis*", Prod. of the XLVIII ETRAN Conference, Čačak, June 6-10, 2004, Vol. 1, pp. 21-24.
97. Zerbe, V., and **Litovski, V.,** "*Design of parallel digital systems and semantic traps*", Prod. of the XLVIII ETRAN Conference, Čačak, June 6-10, 2004, Vol. 1, pp. 91-94.
98. Dimitrijević, M., **Litovski, V.**, Jovanović, S., »*Računarski sistem za izvodjenje laboratorijskih vežbi iz Elektronike***",** V simpozijum industrijska elektronika - INDEL 2004, Banja Luka, ISBN 86-7122-014-1, pp. 156-160.
99. Andrejević, M., **Litovski, V.**, Zwolinski, M., »*ANN application in modeling MEMS***",** V simpozijum industrijska elektronika - INDEL 2004, Banja Luka, ISBN 86-7122-014-1, pp. 99-102.
100. Savić, M., Ađelković, B., and **Litovski, V.**, »*Parallel mixed-mode simulation – Preliminary study***",** V simpozijum industrijska elektronika - INDEL 2004, Banja Luka, ISBN 86-7122-014-1, pp. 76-79.
101. Sokolović, M., Savić, M., **Litovski, V.**, Jevtić, M., Petković, P., "*Testiranje i dijagnostika A/D konvertora integrisanog merača potrošnje električne energije*", Zbornik radova konferencije INFOTEH-Jahorina, Vol. 4, Ref. E-III-7, March 2005, pp. 349-353.
102. Dimitrijević, M. and **Litovski, V.,** "*Implementation of 1MHz Network Analyzer using PC-based Acquisition Card"***,** Zbornik radova XLIX konferencije Etran 2005, Budva, pp.91-94
103. **Litovski, V.,** Andelković, B., "*A Comparative Analysis of Design Languages for Hardware-Software Systems"***,** Zbornik radova XLIX konferencije Etran 2005, Budva, pp. 95-98.
104. Savić, M., Mrčarica, Ž., and **Litovski, V.,** "*Power electronic circuits simulation using ideal switches* ",13th International Symposium on Power Electronics - Ee 2005, XIII Međunarodni simpozijum Energetska elektronika – Ee 2005, Novi Sad, Serbia & Montenegro, November 2nd - 4th, 2005, paper No. T1-1.4, pp1-4.
105. Milojković, J., and **Litovski, V.,** "*End-of-life management of power electrical components*",13th International Symposium on Power Electronics - Ee 2005, XIII Međunarodni simpozijum Energetska elektronika – Ee 2005, Novi Sad, Serbia & Montenegro, November 2nd - 4th, 2005, Paper No. T1-1.7, pp. 1-5.
106. Petković, P., i **Litovski, V.,** "*Koncept integrisanog merača potrošnje električne energije*",13th INTERNATIONAL SYMPOSIUM on POWER ELECTRONICS - Ee 2005, XIII Međunarodni simpozijum Energetska elektronika – Ee 2005, Novi Sad, Serbia & Montenegro, November 2nd - 4th, 2005, Paper No. T4-4.6, pp. 1-5.
107. Sokolović, M. i **Litovski, V. B.**:»*Efikasno određivanje statističkog najgoreg slučaja kašnjenja u složenim digitalnim kolima*», L Konferencija ETRANa, Beograd, Juni 2006. god., pp. EL, 1, 23-26.

108. Andrejević, M., Petrović, V., Mirković, D., and **Litovski, V. B.,:** «*Delay defects diagnosis using ANNs*», L Konferencija ETRANa, Beograd, Juni 2006. god., pp. EL, 1, 27-30.
109. Savić, M., Mrčarica, Ž., and **Litovski, V.**, «*Implementation nonlinear ideal switch model in SPICE*», Zbornik radova 6-tog Simpozijuma Industrijska Elektronika, INDEL 2006, Banja Luka, Novembar 2006, pp. 27-31.
110. Anđelković, B., and **Litovski, V.** «*Parallel transistor level simulation of electronic circuits ona Beowulf cluster*», Zbornik radova 6-tog Simpozijuma Industrijska Elektronika, INDEL 2006, Banja Luka, Novembar 2006, pp. 32-35.
111. Dimitrijević, M., Anđelković, B., Savić, M., and **Litovski, V.,** «*Gradification and parallelization of electronic circuit simulator*», Zbornik radova 6-tog Simpozijuma Industrijska Elektronika, INDEL 2006, Banja Luka, Novembar 2006, pp. 95-100.
112. Sokolović, M., **Litovski, V.**, and Zwolinski, M., «*Fan-out based delay estimation in digital circuits*», Zbornik radova 6-tog Simpozijuma Industrijska Elektronika, INDEL 2006, Banja Luka, Novembar 2006, pp. 101-105.
113. Andrejević, M., and **Litovski, V.,** «*Fault diagnosis in analog part of mixed-mode circuits*», Zbornik radova 6-tog Simpozijuma Industrijska Elektronika, INDEL 2006, Banja Luka, Novembar 2006, pp. 117-120.
114. Milojković, J. and **Litovski, V.,** *«Program uspostavljanja sistema reciklaže otpadne elektronske opreme od kompjutera*», Zbornik radova 6-tog Simpozijuma Industrijska Elektronika, INDEL 2006, Banja Luka, Novembar 2006, pp. 121-126.
115. Anđelković, B., **Litovski, V. B.,** and Petković, P., «*Implementation and performance analysis of parallel circuit simulator on BEOWULF cluster*», 51. konferencija za elektroniku, telekomuniklacije, računarstvo, automatiku i nuklearnu tehniku, ETRAN, Herceg Novi, 04-08 Jun, 2007, Rad. EL1.6
116. Milojković, B., i **Litovski, V. B**., «*Novi postupci predviđanja za potrebe održivog razvoja*», 51. konferencija za elektroniku, telekomuniklacije, računarstvo, automatiku i nuklearnu tehniku, ETRAN, Herceg Novi, 04-08 Jun, 2007, Rad. EL1.8
117. Popović, B., i **Litovski, V.,** «*Podizanje kvaliteta nastave iz elektronike putem unapređenja laboratorijskih vežbanja*», 5. Naučno-stručni skup sa međunarodnim učešćem «KVALITET 2007», Neum, BiH, 06.-09 Jun, 2007, Zbornik radova pp. 641-646. Urednik Safet Brdarević. ISSN 1512-9268.
118. **Litovski, V.,** Milojković, J.,**"***Energijska efikasnost u svetlu direktive EC 32 2005"*, XIV Međunarodni simpozijum Energetska Elektronika, Ee 2007, Novi Sad, Srbija, 07.-09. 11.2007. Paper No. T7-2.1, pp. 1-5.
119. Milojković, J., **Litovski, V.,** »*Ponovna upotreba elektronskih proizvoda i projektovanje za ponovnu upotrebu*«, XIV Međunarodni simpozijum Energetska Elektronika, Ee 2007, Novi Sad, Srbija, 07.-09. 11.2007. Paper No. T7-2.4, pp. 1-5.
120. Dimitrijević, M., **Litovski, V.**, *„Izvor napajanja malih gabarita i velikog faktora snage"*, XIV Međunarodni simpozijum Energetska Elektronika, Ee 2007, Novi Sad, Srbija, 07.-09. 11.2007. Paper No. T1-3.2, pp. 1-4.
121. Milojković, J. i **Litovski, V.B.,** *„Postupci predviđanja za ekološke potrebe"*, Ekoist'08, Zbornik radova simpozijuma Ekološka Istina/Ecological trouth, Juni 2008, Soko Banja, pp. 543-548.
122. Milojković, J. i **Litovski, V.B.**, *„Eko-projektovanje računarske opreme u skladu sa direktivom EC 32 2005"*, ETRAN'08, Zbornik radova LII konferencije ETRANa, Juni 2008, Palić, pp. EL2.1-1-4.
123. Andrejević, Štosović, M., i **Litovski, V.B.,** *„Sinteza hijerarhijskog dijagnostičkog sistema za kola sa mešovitim signalima"*, ETRAN'08, Zbornik radova LII konferencije ETRANa, Juni 2008, Palić, pp. EL2.2-1-4.

124. Litovski, V. and Petković, P.,"*Why The Power Grid Needs Cryptography?*"**,** Zbornik radova VII simpozijuma Industrijska Elektronika - INDEL 2008, Banja Luka, 06.11.-08.11., 2008, pp. 75-81. **Preštampano u Electronics, Vol. 13, No. 1, June 2009, pp. 30-36.**
125. Sokolović, M., Litovski, V., **"***Statistička analiza kašnjenja asinhronih kola primenom logičkog sumulatora*", Zbornik radova VII simpozijuma Industrijska Elektronika - INDEL 2008, Banja Luka, 06.11.-08.11., 2008, pp. 87-92. **Preštampano u Electronics, Vol. 13, No. 1, June 2009, pp. 37-42.**
126. Ćosović, M., i Litovski, V.B., „O jednom konceptu implementacije AES algoritma šifrovanja na FPGA čipu", Zbornik radova VII simpozijuma Industrijska Elektronika - INDEL 2008, Banja Luka, 06.11.-08.11., 2008, pp. 82-86.
123. Milojković, J., Litovski, V., *"Eko-projektovanje elektronske opreme - gubici u standby režimu***",** Zbornik radova VII simpozijuma Industrijska Elektronika - INDEL 2008, Banja Luka, 06.11.-08.11., 2008, pp. 265-269.
127. Dimitrijević, M., **Litovski, V.**, *"Virtual Machine Technology in Grid Computing***",** Zbornik radova VII simpozijuma Industrijska Elektronika - INDEL 2008, Banja Luka, 06.11.-08.11., 2008, pp. 240-243.
128. Milojković, J., **Litovski, V.**, "One step ahead prediction in electronics based on limited information", ETRAN'09, Zbornik radova LIII konferencije ETRANa, Juni 2009, Vrnjačka Banja, pp. EL 1.7-1-4.
129. Milojković, J.B., and Litovski, V.B., "Short-term forecasting of electricity load using recurrent ANNs", *15th International Symposium On Power Electronics – Ee2009*, Novi Sad, Republic of Serbia, October 28th – 30th, 2009, Paper No. T1-1.7, pp. 1-5.
130. Litovski, V., Nieto-Taldriz, O., Zwolinski, M., Trajanov, D., Bojanić, S., Petković, P., and Grnarov, A., „TEMPUS JEP-41107 – System on Chip Design, Overview of the realization", Proc. Of the XVI Conf.: Development Trends, Kopaonik, Serbia, March 2010, pp. 308-311.

Radovi na međunarodnim Konferencijama štampani u izvodu

1. Petković, P., Marković, V., **Litovski, V.**, *"Analysis Of Complex Microwave Circuits Using SPICE"*, Trans Balck Sea Symposium on Applied Electromagnetism, Metsovo, Greece, 17-19. April, 1996.
2. Petković, P., Marković, V., **Litovski, V.**, *"Symbolic Analysis Of Complex Microwave Circuits In Terms Of Power Wave Parameters"*, Trans Black Sea Region Symposium on Applied Electromagnetism, Metsovo, Greece, 17-19. April, 1996.

Radovi na domaćim Konferencijama štampani u izvodu

1. Vacić, Z., Stanković, T., **Litovski, V.**, *"Jedno rešenje automatskog upravljanja i kontrole sistema sa decentralizovanim pogonom"*, Zbornik radova I naučno-stručnog skupa "Specifični problem projektovanja i izrade finomehaničkih uredjaja", Mašinski fakultet, Niš, septembar, 1981.
2. Popović, B., i **Litovski, V.,** "*Koncepti učenja na daljinu primjenjeni na nastavu iz elektronike*", Program Simpozijuma INFOTEH-Jahorina 2008, Elektrotehnički fakultet Sarajevo, p. 51.

Doktorska disertacija

Litovski, V., *"Selektivni filtri s monotonom amplitudskom karakteristikom i konstantnim grupnim kašnjenjem u propusnom opsegu"*, Doktorska disertacija, Elektronski fakultet, Niš, 1977.

Magistarska teza

Litovski, V., *"Novi metodi sinteze selektivnih filtara s monotonom karakteristikom u propusnom opsegu"*, Magistarska teza, Elektronski fakultet, Niš, 1974.

Elaborati i stručne publikacije (tehnička rešenja)

1. **Litovski, V.**, *"Projektovanje C/MOS LSI kola I"*, Grupa autora, Studija, Elektronski fakultet, Usvojilo Naučno veće Instituta EF, 1978, Niš, 1978.
2. **Litovski, V.**, *" Projektovanje C/MOS LSI kola II"*, Grupa autora, Studija, Elektronski fakultet, Usvojilo Naučno veće Instituta EF, 1979, Niš, 1979.
3. **Litovski, V.**, *"Projektovanje C/MOS LSI kola III"*, Grupa autora, Studija, Elektronski fakultet, Usvojilo Naučno veće Instituta EF 1980, Niš, 1980.
4. **Litovski, V.**, Damnjanović,M., *"Projektovanje C/MOS LSI kola IV"*, Grupa autora, Studija, Elektronski fakultet, Usvojilo Naučno veće Instituta EF, 1982), 1982.
5. **Litovski, V.**, Petković, P., *"MOST-program za simulaciju elektronskih kola sa MOS tranzistorima"*, Elektronski fakultet, (Usvojilo Naučno veće Instituta EF, 1984, Preradjeno izdanje štampano 1986), 1984.
6. **Litovski, V.**, Milovanović, D., Damnjanović, M., *"Rezultati istraživanja na projektovanju CMOS IK 1981-1985"*, Grupa autora, Elektronski fakultet, (Umnoženo kao deo izveštaja za istraživački projekt "Mikroelektronske komponente"), Niš, 1985.
7. **Litovski, V.**, Milovanović, D., *"LIFT-program za analizu linearnih elektronskih kola"*, Elektronski fakultet, (Usvojilo Naučno veće Instituta EF, 1984, Preradjeno izdanje štampano 1986), Niš, 1985.
8. **Litovski, V.**, Radenković, T., Radenković, Z., *"SIMGKS - softverski paket koji simulira GKS"*, Grupa autora, deo izveštaja RZNS za projekt "Poluprovodnička mikroelektronika i optoelektronika", Usvojilo Naučno veće Instituta EF, 1986.
9. **Litovski, V.**, Milovanović, D., Stojanović, Z., Milenković, S., *"LIFT II - program za analizu linearnih elektronskih kola sa grafičkim izlazom"*, Grupa autora, Elektronski fakultet, (Umnoženo kao deo izveštaja RZNS za projekt "Poluprovodnička mikroelektronika i optoelektronika"), Niš, 1986.
10. **Litovski, V.**, Petković, P., Milenković, S., Stojanović, Z., *"MOST II - program za analizu linernih kola sa grafičkim izlazom"*, Elektronski fakultet, (umnoženo kao deo izveštaja RZNS za projekt "Poluprovodnička mikroelektronika i optoelektronika"), Niš, 1986.
11. Milovanović, D., Stojanović, Z., Damnjanović, M., **Litovski, V.**, *"Softverski paket za povezivanje logičkog simulatora sa programima za automatsko generisanje topologije"*, Usvojila mešovita komisija TOC, VTI i VP 8634-1, 17 Decembar, 1987.
12. Milenković, S., Milićević, M., **Litovski, V.**, *"Softverski paket za automatski razmeštaj ćelija na čipu GEM 250"*, Usvojila mešovita komisija TOC, VTI i VP 8634-1, 17 Decembar, 1987.
13. Milićević, M., **Litovski, V.**, *"Softverski paket za generisanje PG trake"*, Usvojila mešovita komisija TOC, VTI i VP 8634-1, 17 Septembar, 1987.
14. Damnjanović, M., **Litovski, V.**, Milovanović, R., *"Softverski paket za automatsko povezivanje na GEM 250"*, Usvojila mešovita komisija TOC, VTI i VP 8634-1, 1988.
15. Petković, P., **Litovski, V.**, Stanojević, S., Maksimović, D., Paunović, S., *"Makromodeli složenih logičkih funkcija iz biblioteke ćelija GEM 250"*, Usvojila mešovita komisija TOC, VTI i VP 8634-1, Decembar, 1988.
16. Gmitrović, M., **Litovski, V.**, Ranđelović, Z., Radović, O., Kocić, A., *"Softverski paket za modeliranje veza na GEM 250"*, Usvojila mešovita komisija TOC, VTI i VP 8634-1, Decembar, 1988.

17. Damnjanović, M., **Litovski, V.**, Milovanović, R., *"Softverski paket za automatsko povezivanje na GEM 500"*, Usvojila mešovita komisija TOC, VTI i VP 8634-1, Decembar, 1989.
18. Janković, T., Radenković, Z., **Litovski, V.**, *"Integrisani programski paket za projektovanje gejtovskih matrica"*, Usvojila mešovita komisija TOC, VTI i VP8634-1, Decembar, 1989.
19. Petković, P., **Litovski, V.**, Stanojević, S., Maksimović, D., Paunović, S., *"Makromodeli složenih logičkih funkcija iz biblioteke ćelija GEM 500"*, Usvojila mešovita komisija TOC, VTI i VP 8634-1, Decembar, 1989.
20. Milenković, S., **Litovski, V.**, Đurđanović, O., *"Softverski paket za automatski razmeštaj ćelija na čipu GEM 500"*, Usvojila mešovita komisija TOC, VTI i VP 8634-1, Decembar, 1989.
21. Gmitrović, M., **Litovski, V.**, Ranđelović, Z., Radović, O., Kocić, A., *"Softverski paket za modeliranje veza na GEM 500"*, Usvojila mešovita komisija TOC, VTI i VP 8634-1, Novembar, 1989.
22. Glozić, D., Mrčarica, Ž., **Litovski, V.**, Aleksić, D., *"Alecsis2.0 - hibridni simulator"*, 1993, Elektronski fakultet, (interna publikacija).
23. Glozić, D., **Litovski, V.**, *"ASCOTA3 ADIL - sistem za automatsko projektovanje analognih integrisanih kola"*, 1993, Elektronski fakultet, (interna publikacija).
24. Radenković, T., Radenković, Z., **Litovski, V.**, Aleksić, D., *"ISPGM - integrisani softverski paket za projektovanje polja gejtova na X window platformi"*, 1993, Elektronski fakultet. (interna publikacija).
25. **Litovski, V.**, urednik, *"Nove tehnologije u projektovanju integrisanih elektronskih kola"*, Nauka, Beograd, 1994.
26. Glozić, D., Maksimović, D., Mrčarica, Ž., Dimić, Ž., **Litovski, V.**, *"Alecsis 2.1 Hybrid Simulator Users Manual"*, LEDA, Faculty of Electronic Engineering, University of Nis, Nis, YU, 1994. (interna publikacija).
27. Glozić, D., Mrčarica, Ž., Maksimović, D., Ilić, T., Dimić, Ž, Aleksić, D., **Litovski, V.**, *"Alecsis, The Simulator"*, LEDA, Faculty of Electronic Engineering, University of Niš, Niš, 1996. (interna publikacija)
28. Mrčarica, Ž., Glozić, D., **Litovski, V.**, Maksimović, D, Ilić, T and Gavrilović, D., "Alecsis 2.3 the Simualtor for Circuits and Systems, User's Manual, Elektronski Fakultet (LEDA) Niš, 1998. (interna publikacija)
29. **Litovski, V.B.**, "Itelligent diagnostic systems, preliminary studies", Elektronski Fakultet (LEDA) Niš, 2003. (interna publikacija).
30. **Litovski, V. B.** i ini, "Program uspostavljanja sistema reciklaže otpadne elektronske opreme od kompjutera», Agencija za Reciklažu Republike Srbije, Beograd, 2006.

Nastavne publikacije

1. **Litovski, V.**, *"Zbirka zadataka iz projektovanja elektronskih kola"*, Naučni podmladak, Niš, 1978.
2. **Litovski, V.**, Lazović, S., *"Uvod u elektroniku I deo"*, Institut za naučno-tehničku dokumentaciju Zaštite na radu, Niš, 1981.
3. **Litovski, V.**, *"Projektovanje elektronskih kola pomoću računara"*, Univerzitet u Nišu, 1981.
4. **Litovski, V.**, Petković, P., *"Zbirka zadataka iz projektovanja elektronskih kola"*, drugo dopunjeno izdanje, Univerzitet u Nišu, 1981.
5. **Litovski, V.**, Lazović, S., *"Uvod u elektroniku, II deo"*, Univerzitet u Nišu, 1983.
6. **Litovski, V.**, Radmanović, M., Petković, P., Pavlović, V., *"Praktikum labaratorijskih vežbanja iz fizičkih osnova elektronike"*, Univerzitet u Nišu, 1983.

7. **Litovski, V.**, Lazović, S., *"Uvod u elektroniku, II deo"*, ponovljeno nepromenjeno izdanje, Univerzitet u Nišu, 1988.
8. **Litovski, V.**, Lazović, S., *"Elektronika I, prvi deo"*, Naučna knjiga, Beograd, 1989.
9. **Litovski, V.**, *"CADEC1: Analiza i optimizacija elektronskih kola"*, Naučna knjiga, Beograd, 1989.
10. Lazović, S., **Litovski, V.**, *"Elektronika I, drugi deo"*, Naučna Knjiga, Beograd, 1990.
11. **Litovski, V.**, Lazović, S., *"Elektronika I, prvi deo"*, Nauka, Beograd, 1991.
12. **Litovski, V.**, Petković, P., Milenković, S., Milovanović, D., Glozić, D., Mrčarica, Ž., Maksimović, D., Ranđelović, Z., *"Praktikum laboratorijskih vežbanja iz Elktronike I"*, Nauka, Beograd, 1992, do sada je izdanje ponovljeno četiri puta .
13. **Litovski, V.**, Petković, P., Milovanović, D., Milenković, S., Damnjanović, M., *"CADEC2: Simulacija i projektovanje topologije integrisanih kola"*, Nauka, Beograd, 1992.
14. **Litovski, V.**, Zwolinski, M., *"VLSI Circuit Simulation And Optimization"*, Chapman and Hall, London, 1997.

http://www.amazon.com/gp/pdp/profile/A3HZNQ2LB7R9OH

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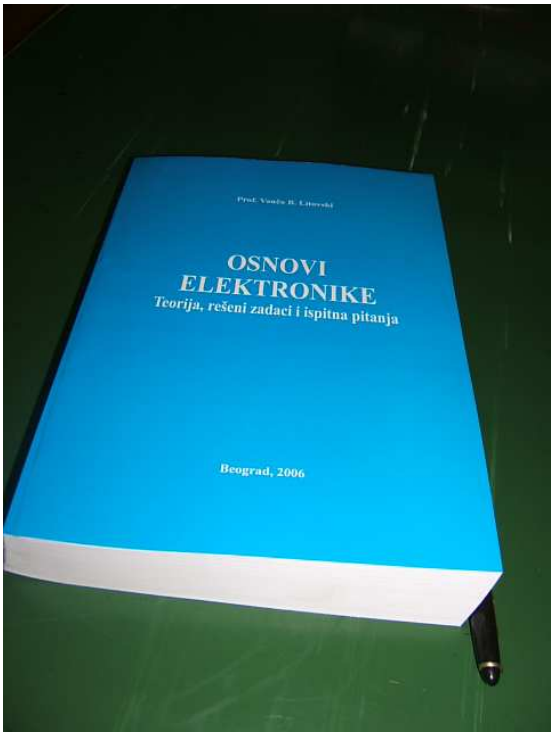
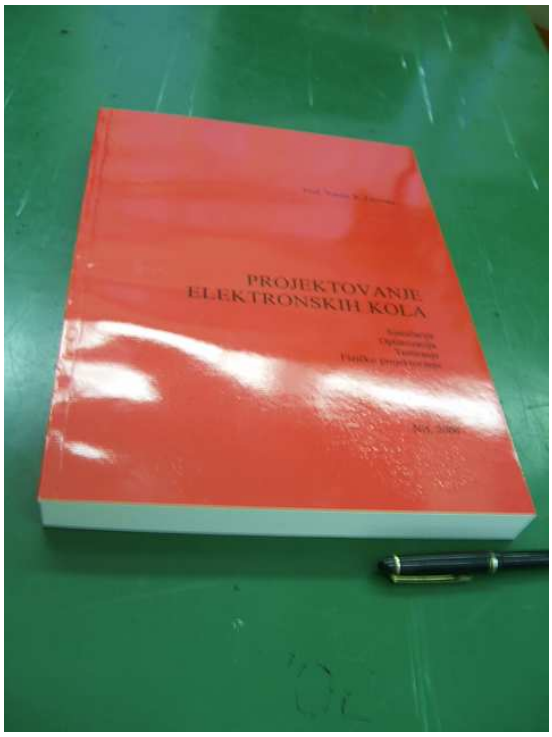
15. **Litovski, V.**, Lazović, S., *"Osonovi elektronike"*, Čuperak Plavi, Niš, 1996. Ponovo štampano 2003 god.
16. Maksimović, D., Janković, S., Milenković, S., Ranđelović, Z., Petković, P., Damnjanović,M., **Litovski,V.**, *"Projektovanje elektronskih kola"*, Laboratorijski praktikum, Elektronski fakultet Niš, 1996.
17. **Litovski, V.,** Milovanović, D., Petković, P., Milenković, S., Randjelović, Z., Panić, V., i Ilić, T., "*Zbornik rešenih zadataka iz osnova elektronike*", Niš, Čuperak Plavi, 1997.
18. **Litovski, V.B.**, "*Projektovanje elektronskih kola, Simulacija, Optimizacija, Testiranje i Fizičko projektovanje*", Nova Jugoslavija, Vranje, 2000.
19. Damnjanović, M, urednik. **Litovski, V.**, Damnjanović, M., Jevtić, M., Milovanović, D., Petković, P., Mrčarica, Ž., Djordjević, G., Maksimović, D., Janković, S., Panić, V., Živković, V., i Leković, B., "*Praktikuma laboratorijskih vezbanja ia projektovanja i testiranja elektronskih kola i sistema*", Elektronski fakultet, Niš, 2000.
20. **Litovski, V.**, *"Osonovi elektronike, Teorija rešeni zadaci i ispitna pitanja"*, Akademska Misao, Beograd, 2006. god. (http://litovski.com/).

21. **Litovski, V.**, "Osnovi testiranja elektronskih kola", Elektronski fakultet, Niš, ISBN 978-86-85195-71-6, 2009.
22. **Litovski, V.**, „Modelovanje komponenata elektronskih kola i sistema", Elektronski fakultet, Niš, ISBN 978-86-85195-75-4, 2009.





Originali knjiga

Prikazi

1. **Litovski, V.**, *"The VHDL Handbook"*, Coehlo, D.R., Journal of Semicustom IC's, Vol. 8, No. 3, Book Rewiew, March, 1991, pp. 53.
2. **Litovski, V.**, *"VHDL: Hardware Description And Design"*, Lipsett, R., Schaefer, C., and Ussery, C., Journal of Semicustom IC's, Vol. 8, No. 3, Book Review, March, 1991, pp. 53.
3. **Litovski, V.**, Pantić, S., *"The Verilog Hardware Description Language"*, Donald E. Thomas and Philip Moorby, Microelectronics Journal, Vol.23, No.4, Book review, July, 1992, pp. 316-317.
4. **Litovski, V.**, Pantić, S., *"Hardware Design And Simulation In VAL/VHDL"*, L.M. Augustin, D.C. Luckham, B.A. Gennart, Y. Huk and A.G. Stanculescu, Microelectronics Journal, Vol.23, No.4, Book review, July, 1992, pp. 316.

Predgovor (knjizi)

Nančeva Filipova, K, et all., “Ispolzovanie na (v) HDL za sintez na elektronenharduer” KING-2001, ISBN 954-9518-21-3

Spisak doktoranata

R. B.	Naslov disertacije	Ime kandidata	Prijavljena	Godina odbrane
1	Makromodeliranje i makroanaliza CMOS LSI elektronskih kola	Predrag Petković		1990
2	Modeliranje i simulacija defekata u CMOS integrisanim kolima modifikovanom konkurentnom metodom	Dragiša Milovanović		1991
3	Novi algoritmi za projektovanje veza u integrisanim kolima tipa GEM	Milunka Damnjanović		1991
4	ALECSIS 2.1 – Objektno orijentisani hibridni simulator	Dejan Glozić		1994
5	Dinamičko učenje neuronskih mreža drugog reda zasnovano na simuliranom očvršćavanju	Srđan Milenković		1996
6	Logička simulacija - procena graničnih svojstava projektovanog digitalnog kola	Maksimović Dejan		2000
7	Novi postupci projektovanja i primene mikrokontrolera u automobilskim aplikacijama	Janković Saša		2005
8	Primena veštačkih neuronskih mreža u dijagnostici elektronskih kola	Andrejević Miona		2006
9	Primena nelinearnog modela idealnog prekidača u simulaciji elektronskih kola	Savić Milan		2007
10	Određivanje statistički najnepovoljnijeg slučaja kašnjenja u digitalnim kolima upotrebom logičkog simulatora	Sokolović Miljana	2007	
11	Paralelizacija i gridifikacija simulatora elektronskih kola i sistema sa mešovitim signalima	Anđelković Bojan	2007	