A Third Order Sigma-Delta Modulator

D. Milovanović, M. Savić and M. Nikolić

Abstract – The design of a sigma-delta modulator is presented in this paper. Third order mash structure is chosen and implemented. Top-down methodology is used and described. Design fulfills imposed requirements which is verified with post-layout transistor level simulation results.

I. Introduction

The use of oversampling sigma-delta modulators in the integration of high-resolution analog-to-digital converters has shown promise for overcoming the analog component limitations inherent in modern VLSI technologies. Sigma-delta modulators employ coarse quantization enclosed in one or more feedback loops. By sampling at a frequency that is much greater than the signal bandwidth, it is possible for the feedback loops to shape the quantization noise so that most of the noise power is shifted out of the signal band. The out of band noise can then be attenuated with a digital filter. The degree to which the quantization noise can be attenuated depends on the order of the noise shaping and the oversampling ratio.

As a part of wider project sigma-delta modulator was designed. It represents an A/D part of a power meter IC. Requirements imposed were: SNDR and dynamic range > 90 dB for maximum input swing of 125 mV differential at 50 Hz. Oversampling ratio is 128 with clock frequency of 524288 Hz which gives bandwidth of 2048 Hz. To fulfill the requirements we chose the third-order modulator. In theory the second-order modulator is sufficient [1], but the third-order will give enough margins for circuit non-idealities and process variations. The modulator comprises a cascade of a second-order stage, hereafter referred as a 2-1 architecture. A cascaded architecture was adopted primarily for two reasons. First, cascading first and second-order modulators eliminates the stability problems associated with third and higher order single stage modulators while retaining essentially the same quantization noise performance [2]. Second, any baseband noise tones produced in the second-order stage are largely suppressed by the succeeding first-order, and the remaining quantization noise is nearly white. The 2-1 architecture is preferable to alternative cascaded third-order architectures because it is less sensitive to component mismatch.

This paper is divided into following parts. Section II and III describes implementation of 2-1 architecture. In section IV behavioral simulation is done to verify architecture implementation. Finally, in section V design of an experimental third-order modulator are given.

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II. Modulator design

The 2-1 architecture is implemented by combining three summing integrators with two comparators and two 1-b D/A converters, as shown in Fig. 1 [3]. The most important building block in this architecture is a summing integrator, for which the output w is the delayed integration of a weighted sum of inputs v_m. In the time domain, the output is

$$w((n+1)Ts) = w(nTs) + \sum_m a_m v_m(nTs) \tag{1}$$

where Ts is the modulator's sampling period. The z transform of the output is

$$W(z) = \frac{z^{-1}}{1-z^{-1}} \sum_m a_m V_m(z) \tag{2}$$

where $V_m(z)$ is the z transform of $v_m(nTs)$

The remaining building blocks in the analog portion of the modulator are comparators and 1-b D/A converters. The comparator circuits acts as a 1-b A/D converters that map their inputs into one of two digital output codes. The two digital output codes are then mapped back into analog levels by the D/A converters. If the two output codes of the comparators are defined as ±1/2, then the D/A converters, neglecting D/A errors, can be represented simply by gain block.

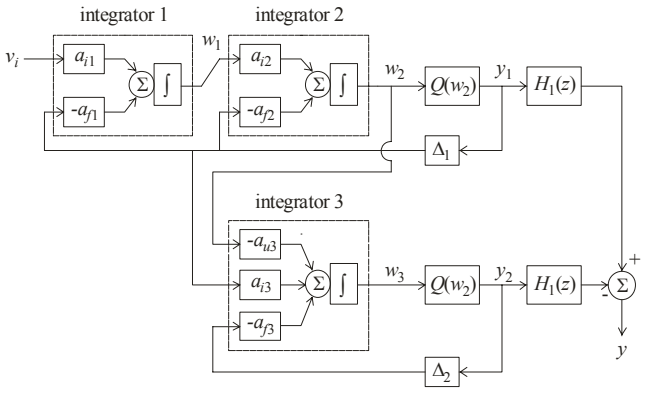

Fig. 1. 2-1 architecture implementation

Digital part of modulator consist of error cancellation filters $H_1(z)$ and $H_2(z)$, which eliminates error from first stage of modulator. In z domain transfer function of $H_1(z)$ and $H_2(z)$ are [3]

$$H_1(z) = \frac{1}{2} z^{-1}(1 + z^{-1}) \tag{3}$$

$$H_2(z) = 2(1 - z^{-1})^2 \tag{4}$$

The integrators' gains used in this design are summarized in Table I [3]

TABLE I
INTEGRATOR GAIN VALUES

Gain	a_{i1}	a_{f1}	a_{i2}	a_{f2}	a_{u3}	a_{i3}	a_{f3}
Value	1.0	0.2	0.5	0.25	0.5	0.1	0.1

III. The Integrator Architecture

Switched-capacitor integrators are used in this design. Two main sources of noise in switched-capacitor integrator are: thermal noise from the amplifier and equivalent kT/C noise resulting from the integrator switches, and flicker noise from the amplifier. The thermal noise is limited by using sufficiently large capacitors to restrict the noise bandwidth. Minimum value used for capacitors in first integrator is 5 pF (C_{REF}). The flicker noise is attenuated using the correlated double sampling topology shown in Fig. 2 [4].

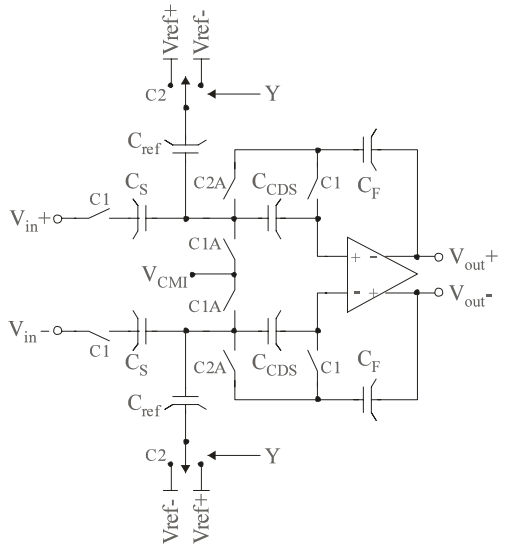

Fig. 2. Correlated double sampling integrator

In the double sampling integrator, a nonoverlapping two-phase clock is used. Switches c_1 and c_{1A} conduct during first clock phase, and switches c_2 and c_{2A} conduct during the second clock phase. Switches c_{1A} and c_{2A} are opened slightly ahead of switches c_1 and c_2 respectively to reduce signal-dependant charge injection onto sampling capacitors C_S [5]. During the first phase, the input V_I is sampled across C_S and amplifier offset is sampled on C_{CDS}. In the second clock phase a charge proportional to the input voltage V_I minus feedback voltage V_{ref} is transferred from C_S and C_{ref} to C_F, while dc offset and flicker noise of the amplifier are cancelled by the voltage stored on C_{CDS}. For proper operation, C_{CDS} must be much larger then input capacitance of the amplifier. In this design C_{CDS} is chosen to be 5 pF.

IV. Behavioral Simulation

The analog circuit block cannot precisely perform their ideal function, so most of modulator nonidealities must be taken into account. Such are sampling jitter, kT/C noise, and operational amplifier parameters (white noise, finite dc gain, finite bandwidth, slew rate and saturation voltages). Only the first integrator needs to be simulated with nonidealities, since their effects are not attenuated by noise shaping. For architecture implementation in Fig. 1 a simulation in Matlab Simulink environment was performed. Ideal modulator output spectrum for a 50 Hz 125mV sinusoidal input signal is shown in Fig. 3.

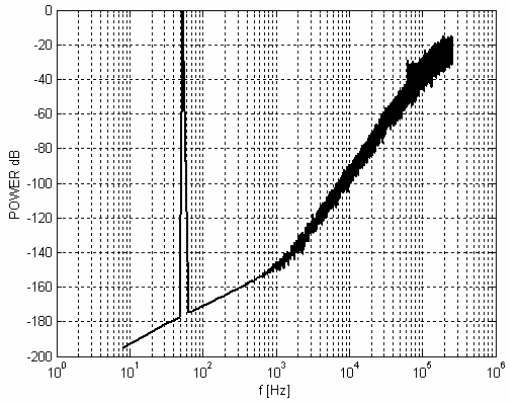

Fig. 3. Ideal modulator's output spectrum

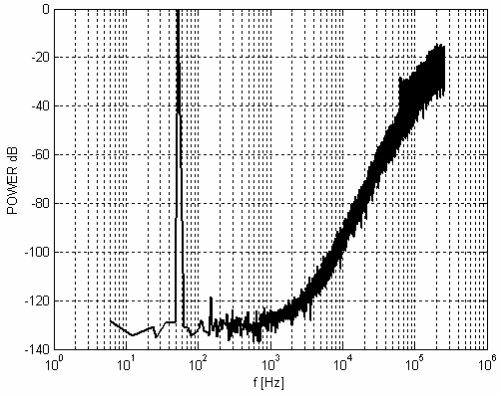

Fig. 5. Output spectrum with nonidealities

Simulink model used to simulate nonidealities is shown in Fig. 4 [6]. Table II gives modulator parameters and values used in simulation. Only white noise is considered, while flicker noise and dc offset are neglected, because first integrator has correlated double sampling. Output spectrum for the same signal of the modulator with modeled nonidealities is shown in Fig. 5.

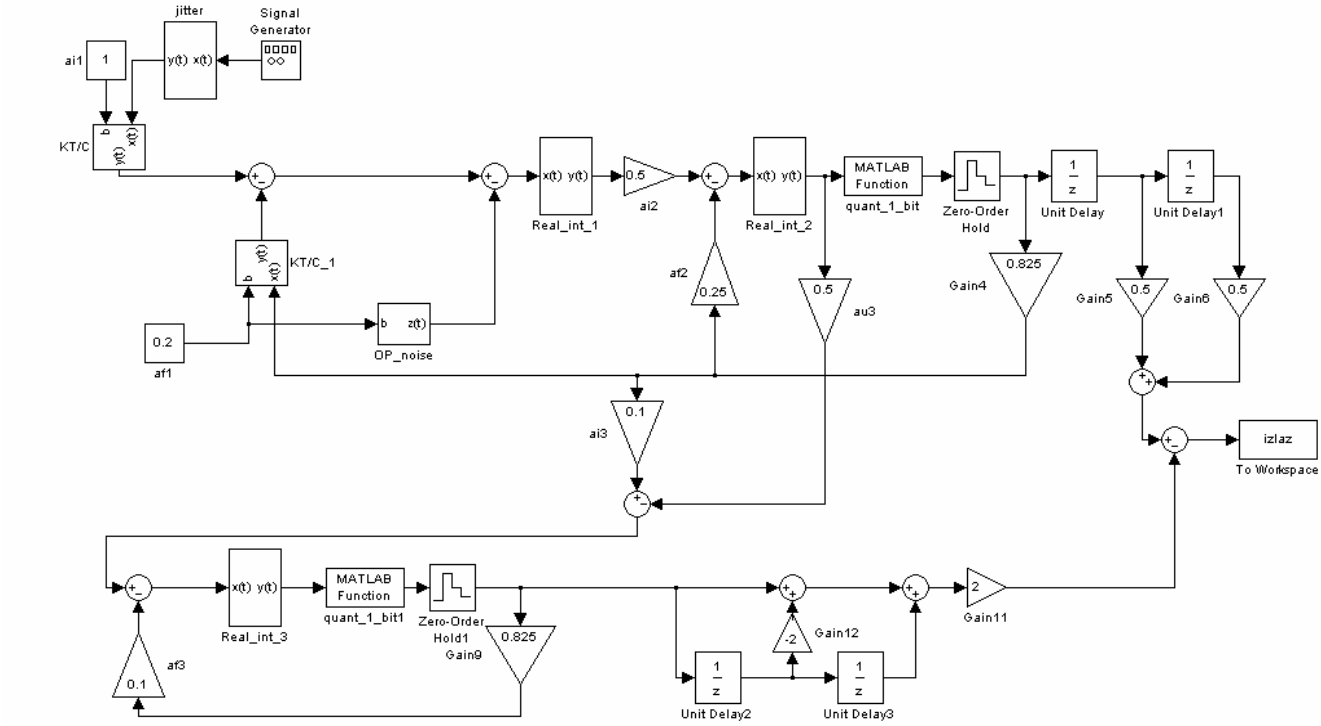

Fig. 4. Simulink model

TABLE II
MODULATOR NONIDEALITIES

Modulator parameter	Value
Sampling jitter	20 ns
Switches (kT/C_S) noise	25 pF
Input-referred operational amplifier noise (thermal)	70 μV_{rms}
Finite dc gain	10^3
Finite bandwidth	2.5 MHz
Slew-rate	4 V/ μs

V. CIRCUIT DESIGN

After behavioral level simulations we had enough parameters for transistor level implementation. All required analog blocks (operational amplifiers, bandgap reference, switches, capacitors and quantizer) were designed, simulated, and then layout is carried out.

The sigma-delta modulator depicted in Fig. 1 was designed for fabrication in 0.35-μm CMOS technology. The operational amplifier used in integrators is the most critical element of the modulator. Behavioral simulation with nonidealities indicates that a slew rate of 4 V/μs, bandwidth of 2.5 MHz is sufficient to meet performance objectives. Since the comparator can be designed to be quite fast, the settling speed of the integrator ultimately limits the achievable sampling rate of the modulator, even if complete settling is not required. The need for high speed, coupled with a relatively modest gain requirement of 60 dB to suppress harmonic distortion, encouraged the use of a single-stage amplifier [7].

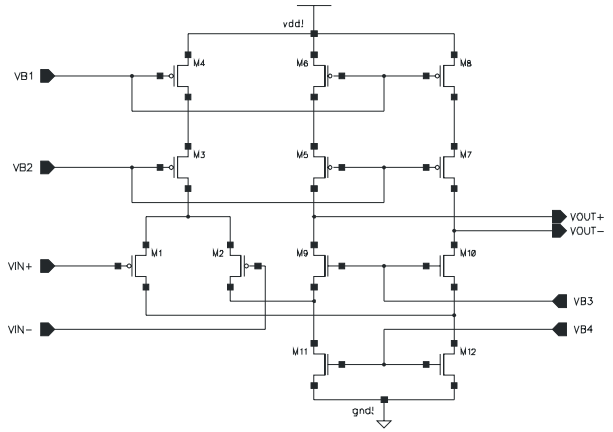

Fig. 6. Folded cascode op-amp

Figure 6 shows fully differential folded-cascoded operational amplifier used in design. The common-mode

levels in the fully differentially amplifier are set by the common-mode feedback circuit shown in Fig. 7. Bias voltages are provided by a wide-swing cascode current mirror bias circuit.

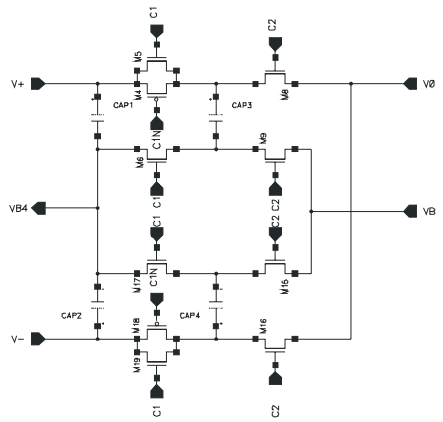

Fig. 7 CMFB circuit

Output spectrum obtained from transistor level simulations data for 8 kHz 125mV sinusoidal input signal is shown in Fig. 8. Input signal frequency is 8 kHz which is enough to have a reasonable simulation time, while giving enough samples (16 k samples) to perform a FFT. In Fig. 9 is shown layout of the modulator. Modulator occupies 0.66 mm^2

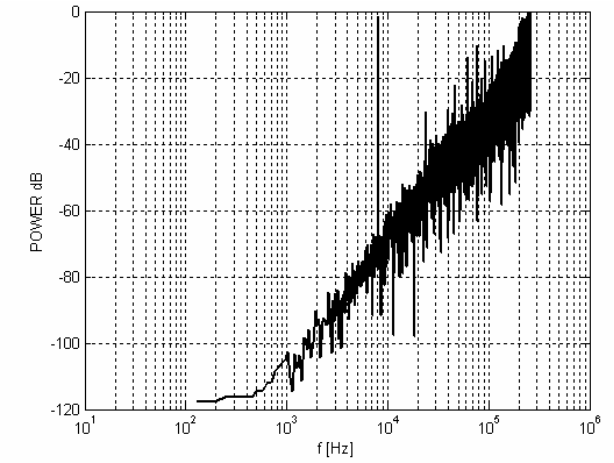

Fig. 8. Output spectrum from transistor level simulation

VII CONCLUSION

In this paper, a 2-1 cascaded sigma-delta modulator design has been described. Transistor level simulation results show that the designed circuit fulfills the imposed requirements. Modulator is designed using Cadence Design System and AMI Semiconductors CMOS 0.35 μm (C035-2P5M-AS) technology. Currently chip is in fabrication phase.

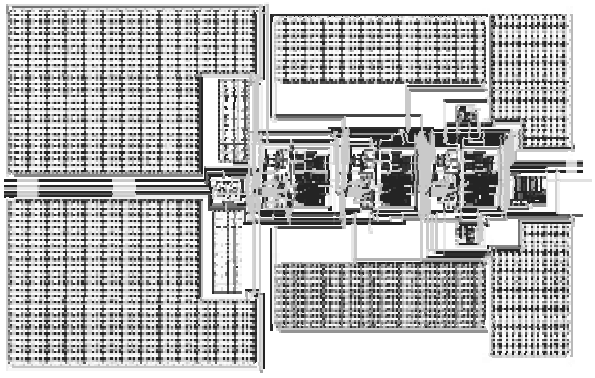

Fig. 9 Layout of the modulator

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