CMOS BANDGAP VOLTAGE REFERENCE

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Abstract – *This paper presents an example of the CMOS bandgap voltage reference design. Proposed circuit is evaluated with a set of simulations. Simulation results show the circuit performance. Circuit exhibits the nominal temperature coefficient of 6 ppm/℃, and dc power supply rejection of 130 dB.*

1. INTRODUCTION

Analog circuits incorporate voltage and current references extensively. Such references are dc quantities that exhibit little dependance on supply and process parameters and a well-defined dependance on the temperature.

As a part of the wider project, a bandgap voltage reference for supplying ADC is being designed. Most important requirement is that temperature coefficient should be less than 50 ppm/°C, preferably 25 ppm/°C, for temperature range -40 to 80 °C. Other requirements are: high PSRR and small chip area. Standard CMOS process is used (Alcatel Semiconductors CMOS 0.7 μm C07MA), where only vertical PNP bipolar transistor is available.

This paper is organized as follows. Section 2. discusses the concepts used in this design. Section 3. describes the proposed circuit. Simulation results are presented in Section 4.

2. DESIGN OBJECTIVES

The overall objective of designing a precision reference is to achieve high accuracy over all working conditions. Most important are: temperature variation, process variation and supply variation. Concepts of reducing the impact of those variations on reference voltage deviation, which were used in the proposed circuit, will be explained in the following.

The base-emiter voltage of bipolar transistor or, more generally, the forward bias voltage of a pn-junction diode exhibits negative temperature coefficient (TC). On the other hand, two bipolar transistors that operate at unequal current densities, exhibit difference between their base-emitter voltages that is directly proportional to the absolute temperature. Using these negative- and positive-TC voltages, a reference having a nominally zero temperature coefficient can be developed.

Well known simple PTAT (Proportional To Absolute Temperature) current generator topology is shown in Fig. 1. [1]. This circuit has a zero-current quiscent state. In order to avoid this state, a start-up cicuit is requiered. The output current of this circuit is very power supply voltage dependant. This can be reduced by using cascode current mirrors. Voltage difference between nodes X and Y is the most common source of inaccuracies. In order to avoid this, an operational amplifier can be used, with X and Y as inputs, as shown in Fig. 2. Here, PTAT the voltage, equal to $I_{\text{out}} R_2$, is added to the base-emitter voltage (negative-TC), providing voltage with nominally zero temperature coefficient.

The output voltage equals:

$$V_{\text{ref}} = V_{\text{BE3}} + (R_2 / R_1) \cdot V_{\text{T}} \cdot \mathbf{ln}n \qquad (1)$$

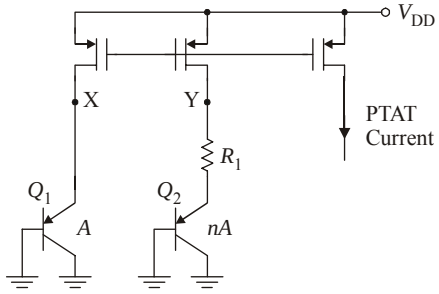

Fig. 1: *Simple PTAT current source*

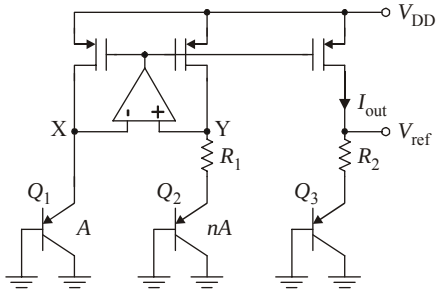

Fig. 2: *Simple bandgap voltage reference*

This reference is first-order voltage reference, because the PTAT cancels only the first-order term in the polynomial approximation that represents relationship between the diode voltage and temperature.

By adjusting the circuit elements, the value of the TC at room temperature can be set to zero. [1]

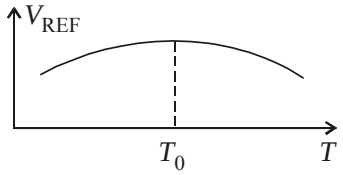

Fig. 3: *Temperature dependence of a bandgap voltage*

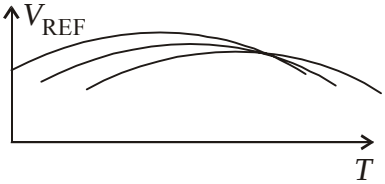

Fig. 4: *Variation of the zero-TC temperature for different samples*

Process variations have great impact on bandgap voltage deviation. Figure 4. presents the variation of the zero TC temperature for different samples (different process parameters). Trimming techniques offer the solution to this problem [2]. For the circuits with trimming network, PTAT current can be adjusted after fabrication. Voltage variations can be minimized by careful layout design. Namely, special attention should be paid on matching of the current mirror devices, resistors (R_1 and R_2 in Figure 2.) and BJTs.

Supply voltage variations, both dc and transient noise, result in reference voltage deviation. Line regulation performance refers to the steady-state voltage changes in the reference resulting from dc changes in the input supply voltage. The robustness and the stability of the circuit with respect to the power supply noise are defined as the power supply rejection (PSR). Though PSR refers to small-signal response, the general techniques used to improve line regulation will enhance PSR as well. [2]

The basic concept behind improving PSR and line regulation performance is increasing the effective impedance from sensitive nodes (especially the reference voltage) to the input power supply voltage. Therefore, cascodes can therefore be used for this purpose. Another method of improving PSR is relayed on preregulating the input voltage.

Figure 5. illustrates one concept of regulated supply. The idea is to generate a local supply, V_{DDL} , which is defined by a reference V_{R1} and the R_{r1}/R_{r2} ratio and hence relatively independent of the global supply voltage. [3]

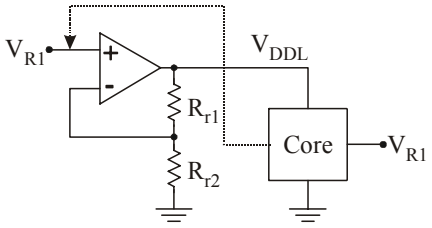

Fig. 5: *Regulation of the supply voltage of the core to improve supply rejection.*

3. PROPOSED CIRCUIT

Proposed circuit is shown in Figure 6.

Bandgap core is the same as the one presented in Figure 2. Startup circuitry is added to ensure that output voltage and regulated supply do not remain at ground when power is applied. On startup, MOS transistor MS5 forces current into the collector of the Q1. This ensures that the circuit avoids the zero-current state. While reaching the stable state of operation, the gate voltage of MS2 rises, and turns it on. As a result, gate voltage of MS4 decreases and turns off current through MS4, MS3 and MS5, driving the bandgap core into desired state of operation.

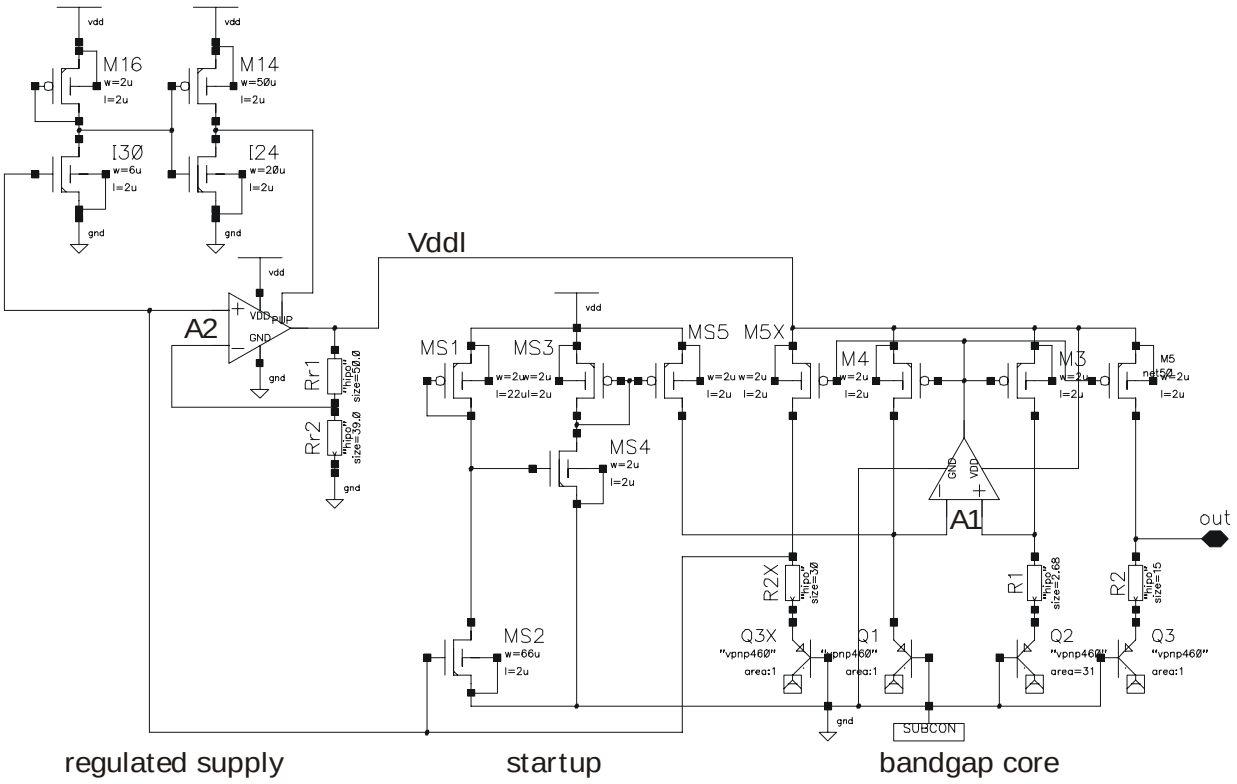

Fig. 6: *Bandgap reference*

Amplifier A2 together with Rr1 and Rr2 provides regulated supply as shown in Figure 5. Figure 7. presents the detailed circuitry of A2. This amplifier is similar to [4], with the addition of the power-up (PUP) port. When a high voltage is applied to this port (gate of M0) it forces the amplifier output to V_{DD}. This is used during startup, providing the desired state of operation. Regulated supply startup can be described using Figure 6. The voltage from within the core controls the operation of the I30. On startup, I30 is turned off, which forces the PUP signal to go low, providing the normal operation of the A2.

It is essential that A2 amplifier does not operate in saturation. Also, during startup the circuit may oscillate because the change of the PUP signal causes local supply drop, which in turn may turn off the I30 device and change PUP to previous state. This problem can be solved by careful design of the regulated supply circuitry.

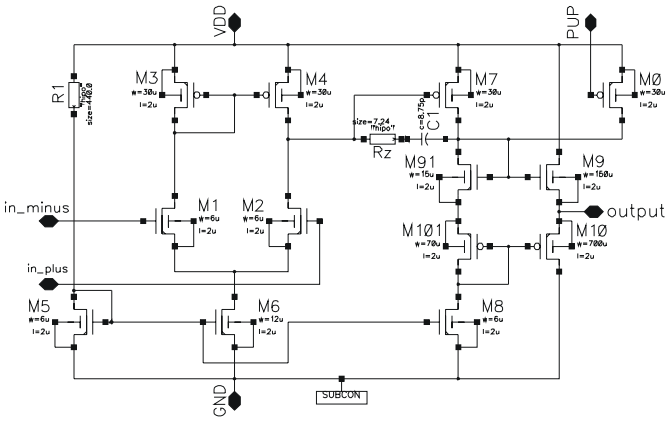

Fig. 7: *Amplifier used in the regulated supply circuit*

4. CIRCUIT PERFORMANCE

In order to assess the circuit performance a set of simulations was performed using the Spectre simulator and the Affirma Analog Environment [5]. All the device models correspond to the target technology.

Figure 8. shows the temperature variation of the bandgap voltage. The circuit provides referent voltage of 1.1486 V at 27 °C with temperature coefficient of 6 ppm/°C.

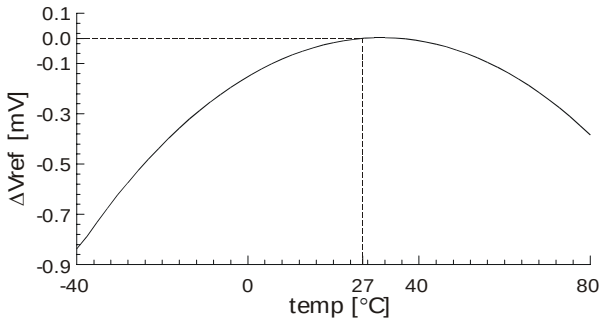

Fig. 8: *Referent voltage variation with temperature.*

In order to estimate the impact of the process variations, the corner analysis [6] was performed. Corners represent various combinations of extreme process parameters values. Sixteen corners, which were predefined for the given technology, were simulated. Figure 9. presents the corner analysis results. Temperature coefficients for the various corners vary from 5 to 580 ppm/°C. Referent voltage on the room temperature vary from 1.14 to 1.19 V. Corner process parameters present extremes, and therefore give rather pessimistic prediction when compared to the fabricated circuits. It can be noted that the implementation of trimming network would greatly reduce the additional temperature variation induced by the process variations. On the other hand, it would consume additional area and introduce more complex testing procedures. The variation of the nominal reference voltage can be circumvented with the calibration of the digital part of the system for which this bandgap is designed, so it does not present a problem.

And finally, the PSR performance simulations were performed. Figure 10. presents the PSR variation with respect to frequency. The implemented regulated supply greatly improved the PSR of the circuit. Without the regulated supply, dc supply rejection ration was only 10 dB. It can be noted that this circuit provides a dc power supply rejection ratio of 130 dB. The addition of the output off-chip 0.1 μF capacitor would greatly improve the PSR performance over higher frequencies.

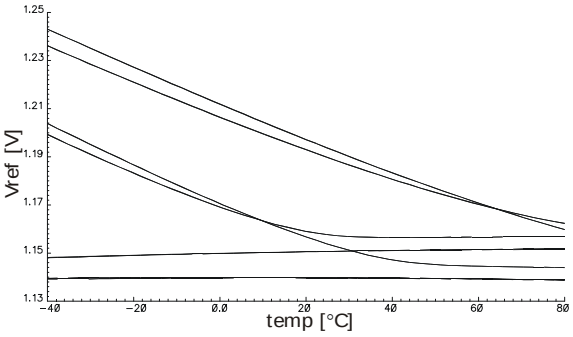

Fig. 9: *Corner analysis results*

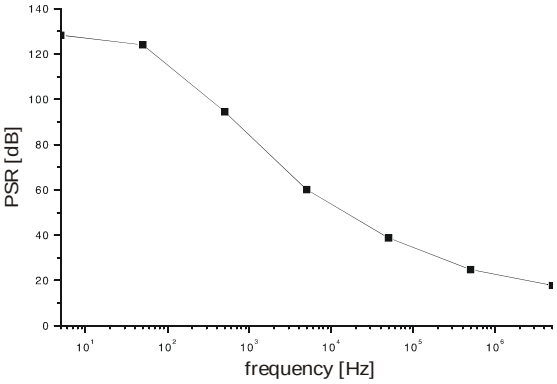

Fig. 10: *Power supply rejection*

5. CONCLUSION

Proposed circuit fulfills the imposed requirements. It exhibits the nominal temperature coefficient of 6 ppm/°C and dc power supply rejection of 130 dB according to performed simulations. Corner analysis shows the great impact of the process variations on the circuit performance. This can be reduced with implementation of the trimming network.

REFERENCES

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[5] -, Cadence 2002 IC 4.46 Package Documentation.

[6] V. B. Litovski, “Projektovanje elektronskih kola: simulacija, optimizacija, testiranje, fizičko projektovanje”, Nova Jugoslavija, Vranje, 2000. (in Serbian)

Sadržaj – U ovom radu predstavljeno je kolo CMOS bandgap referentnog izvora napona. Predloženo kolo procenjeno je pomoću niza simulacija. Kolo ispoljava nominalni temperaturski koeficijent od 6 ppm/°C i potiskivanje varijacije jednosmerne komponente napona napajanja od 130 dB.

CMOS BANDGAP REFERENTNI IZVOR

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