DESIGN FOR TESTABILITY IN AN APPLICATION SPECIFIC DSP

Miljana Sokolović, Predrag Petković
Department of Electronics, Faculty of Electronic Engineering, Beogradska 14, 18000 Niš
miljana@ elfak.ni.ac.yu; predrag@ elfak.ni.ac.yu

Abstract. *During large DSP systems on chip design, one of the most important demand is assigned to fast and efficient testability as well as the ability of defect diagnostics. This is very important considering expenses and time consumption needed for circuit design and potential design faults allocation. This paper presents an original practical testing problem solution in a specific application DSP chain dedicated for integrated power-meter, that benefits BIST and scan testing and faults allocation techniques in a digital circuits. Practical application of the proposed solution is confirmed by VHDL simulations.*

1. INTRODUCTION

The aim of electronic circuit testing is to determine whether the fabricated component, block or system operates well or not. But the velocity of design and manufacturing, inflicted by market, irrevocably leads to omissions that should be solved as fast as possible. If defects detecting and locating task would be faster and easier, fabrication expenses would be significantly smaller and the fabrication process faster. Defect diagnostics is essential, especially in test chip fabrication. Therefore, it is not just important to determine if the systems functionally fulfils all requirements, but also to discover where and why the problem occurs. In early design and fabricating phases, particularly in prototypes and test chip designs, a special attention is paid to diagnostics. As the design and fabrication of test versions goes on, the accent is moving from diagnostics to electronic circuits testing.

On the other hand, significant numerosity, variety and complexity of DSP systems, require the use of some universal testing technique that can be applied to all DSP chain building blocks, regardless to the function they perform. Design For Testability (DFT) and Built In Self Test technique (BIST) principles are inflicted as general solutions of this problem.

This paper presents one DSP chain testing method. This DSP chain is a part of integrated circuit used in power consumption measurement. The function of the DSP discussed is calculation of all relevant variables referred to the energy metering, based on instantaneous values of voltage and current in digital form.

The paper is organized as follows. The next section describes general principles of DFT, BIST and boundary scan BS. Thereafter, a special attention will be paid to a particular application specific DSP chain. An original testing approach of such DSP system that benefits BIST and scan principles will be described next.

A complete logic that the testing method is based on, is described and simulated in VHDL. In this way, a functionality of the solution described as well as its universality of applying to any other DSP chain is confirmed. At the end simulation results will be shown.

2. DFT, BIST AND BS TESTING PRINCIPLES

In general, DFT presents a circuit design that enables efficient circuit testing with the ability of detecting as many faults as possible. The most often and the simplest approach is incorporating an additional test logic that can increase controllability and opservability. However, this method is not suitable for very large integrated circuits, where regardless to the big number of pins, some more, used just for testing, have to be added. Partial solution of this problem can be the use of additional multiplexers, as shown in Figure 1. Using them, primary inputs (PI) and primary outputs (PO) are added an alternative tasks related just to testing [1].

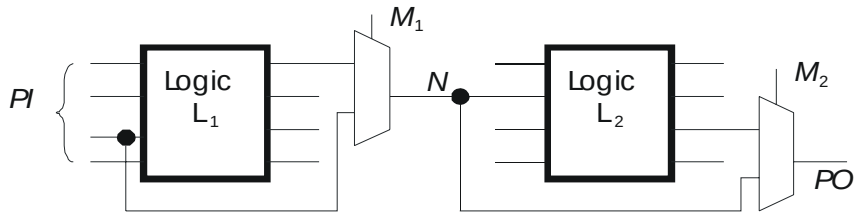

Figure 1. *Increasing controllability and opservability without increase the number of external pins*

One control pin (M_1) can select a various number of internal points (of the logic L_2), to isolate them from their usual stimulus, and to connect them directly to primary inputs. The second control signal (M_2) enables the connection between various number of primary inputs and internal points (the outputs of the logic L_2). This concept can offer two operating modes:

1. normal operating mode (M_1M_2=00);
2. testing L_1 – value at node N is transferred to the primary output (M_1M_2=01)
3. testing L_2 – value at node N is controlled by the signal at the primary input (M_1M_2=10)

The efficiency of the proposed DFT method depends on the ability to isolate all testing blocks in the testing phase. It is usual to perform I/O operations using the serial port in order to minimize the number of input/output pins dedicated for testing.

Built In Self Test (BIST) is based on incorporation of test functions into a chip [1], [2]. This approach can overdo one big drawback. That is the difference between internal and external bandwidth. Architecture of the chip that is based on this technique is shown in Figure 2. External NF signal controls testing, and special internal cells generate test signals and collects the information about their response.

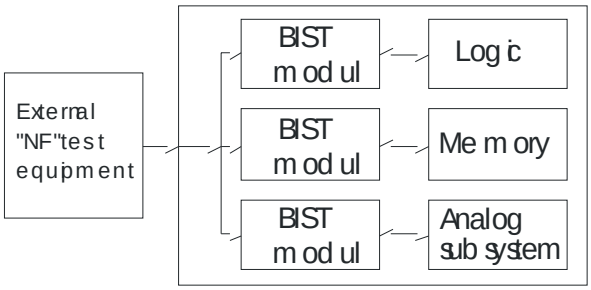

Figure 2. *Architecture of the BIST chip*

The IEEE standard 1149.1 defines BS method. This standard assumes an additional built in test logic that simplifies the system logic testing as well as the environment testing [3], [4]. A chip realized according to this standard consists of

system logic that performs its primary function, and additional test logic as shown in figure 3.

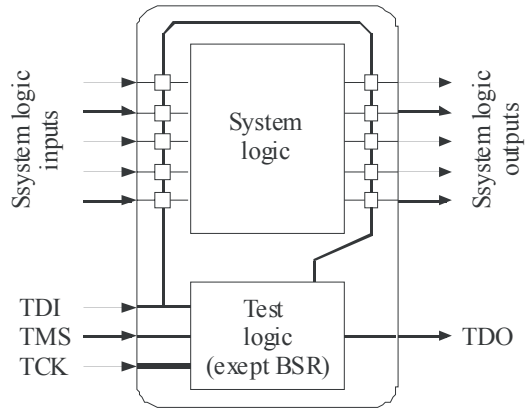

***Figure 3**. The structure of an IEEE 1149.1 standard based chip*

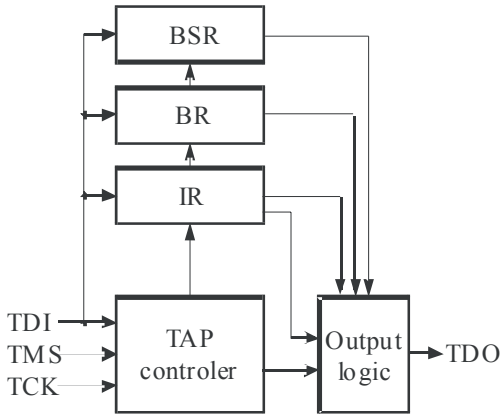

***Figure 4**. Block diagram of the test logic*

Figure 4 shows building blocks of the test logic: boundary-scan register (BSR), bypass register (BR), instruction register (IR), TAP (test access port), controller and output logic. BSR is an array of BS cells (BSC) and can be serially written and read. BSCs are memory elements placed on the boundary of an integrated circuit. A signal from the primary input must go through one BSC in order to reach the system logic. Similarly, a signal from the output of the system logic must go through one BSC in order to reach a primary output.

Watched from the outside, a chip based on this standard has four additional pins. Namely these are TDI – Test Data In, TDO – Test Data Out, TMS – Test Mode Select and TCK – Test Clock. All of them form a port for testing called Test Access Port (TAP).

Existing so many different testing principles implies that none of them is ideal.

DFT method requires additional testing pins, which increases the chip area. Using serial port relaxes this problem, but in turn, reduces testing speed.

The main disadvantage of BIST technique occurs in large circuits, because they inevitably increase the testing block size. Similar observation stands for the BS method although a serial port can also be assumed as a disadvantage.

All described techniques suffer of diagnostics disability. In the scope of chip prototyping this becomes a serious disadvantage.

3. **DSP** CHAIN IN AN INTEGRATED POWER-METER

Let us consider one of DSP chain solutions used within electronic energy metering devices. It assumes a set of operations needed for active (P), reactive (Q) and apparent power (S) calculations together with power factor (PF) and current and voltage root mean square values (I_{rms} and V_{rms}) computation [5]. This chain is shown in Figure 5.

Input signals are digital values of instantaneous voltage and current. These data are processed through a set of arithmetic operators, as indicated in Figure 5. Actually, DSP consists of several chains having unique origin.

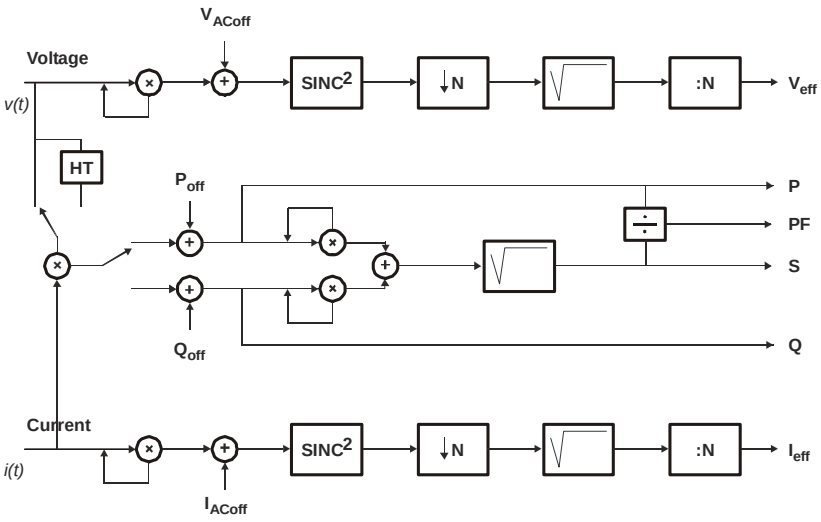

Figure 5*. DSP chain*

Calculation of I_{rms} and V_{rms} is performed according to the definition of the root means square value for the time dependent signal *x(t)* in discrete form:

$$X = \sqrt{\frac{1}{T}\sum_{i=1}^{N} X^2(i)}. \qquad (1)$$

Second part of this chain is used for calculation of P, Q, S and PF. Additional circuit blocks here are Hilbert transformer (HT), as well as digital dividing block. Active power is determined as a DC component of the product of instantaneous voltage and current, while the reactive power is determined in the same manner, after the voltage is processed within HT. Using these two results, the apparent power as well as the phase factor can be calculated in the following way:

$$S = \sqrt{P^2 + Q^2}\,, \qquad PF = P/S \qquad (2)$$

Considerable hardware savings are gained using the same functional blocks for more operations (for example, multiplying and adding). All DSP chain building blocks are connected in series, without any feedbacks and loops. This fact simplifies testing and diagnostics processes. The principle of built-in test logic will be described in detail in the following section.

4. TESTING AND DIAGNOSTICS PRINCIPLES IN AN APPLICATION SPECIFIC DSP

A concept of described DSP chain testing is illustrated in Figure 6. It is based on each operation block scanning. A chip has four operating modes. Two modes of interest are normal function and testing mode. Testing mode offers two kinds of testing. One is global testing and the other is detail testing. Testing logic consists of comparators, data registers (which are also used in a system logic) and a *signature register*. The aim of the test is to determine whether the operator block functions well. Each operator keeps operands data in appropriate input registers while the result is stored in the output register. After processing, the obtain output is compared with the desired one. If the results match, the appropriate bit (corresponding to the operator under test) in signature register keeps flag "1". However, registered malfunction sets the bit to "0". Ones written "0" on a certain bit position, cannot be overwritten with another value until the signature register is read.

A described concept presents a global testing. It means that the process of global testing consists of two phases. The first one is loading the test vectors and expected response for every block. Then confirmation phase takes place. This concept fulfills both demands, for fast testing and diagnostics.

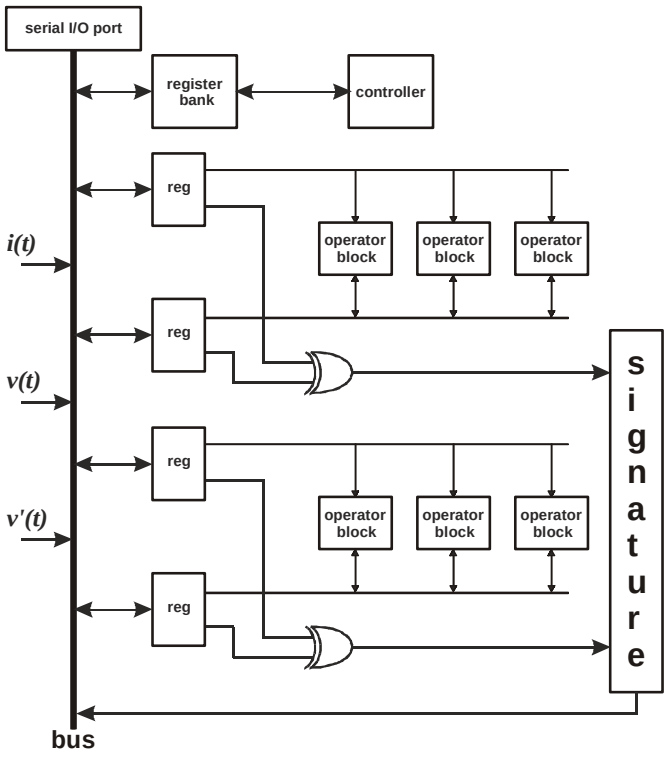

***Figure 6**. Testing and diagnostics concept of DSP chain*

Besides, this testing concept allows a detailed testing. If a malfunctioning of one operator block is detected, the logic enables the direct approach to this operator using bus connection to serial I/O port. Therefore, it allows opservability of detected fault.

The presented DSP testing and diagnostics concept offers following advantages comparing to the standard testing techniques:

- ***minimal enlargement of the system logic on chip,***
- ***simple realization,***
- ***universality that is the use on the other DSP chains,***
- ***fast testing and***
- ***fast defect detecting and locating .***

Considering all issues, it should be kept in mind that this concept has a primary application in a test chip and prototyping where number of design and fabrication irregularities is expected.

5. VHDL DESCRIPTION OF THE TEST LOGIC AND ITS SIMULATION RESULTS

All blocks needed for the test logic are described in VHDL as Figure 7 indicates. The length of all input/output digital words for each test block is defined as a generic in order to reuse the same description for different circuits.

The main goal of the proposed concept is the improvement of diagnostic abilities, since the output result does not give the response of the block. Instead, one gets information which block doesn't function well. A reasonable question is why some BS logic elements haven't been used. The answer is that BS-like solution requires double more number of latches or flipflops for inputs and outputs of each block. Instead, in the proposed solution, one register can be used as input or output storage element. Considering the traces testing, in this moment, drastic errors are not expected in the design here, because the routing process will be done automatically using the adequate circuit design tool.

After automatic VHDL code generation, Active HDL simulator [6] has been run. An array of test vectors have been specified, in order to confirm the functionality of the proposed structure.

Figure 8 shows the simulation results. After loading test vectors into data registers, and obtaining the appropriate response, a comparison is performed. The primary function of the test logic is verified. In the case of disparity of two digital words (the real result of the block and the expected result) the corresponding bit position in the signature register is properly flagged. This bit position keeps the value in the case of irregularity detection. It means that there is no result overwriting. According to the bit position in a signature digital word, one can determine which one of the operator blocks does not function well.

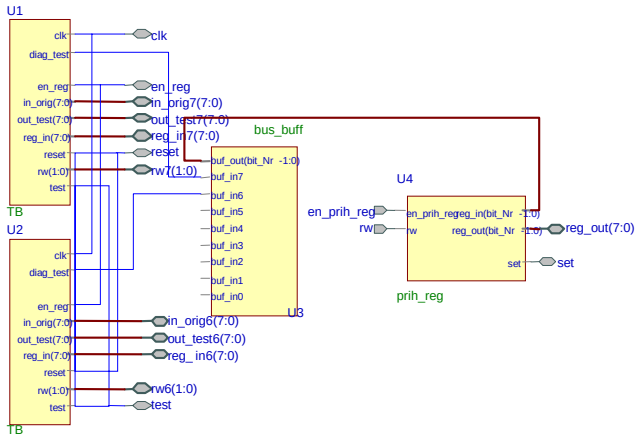

***Figure 7**. Testing and diagnostics concept of DSP chain*

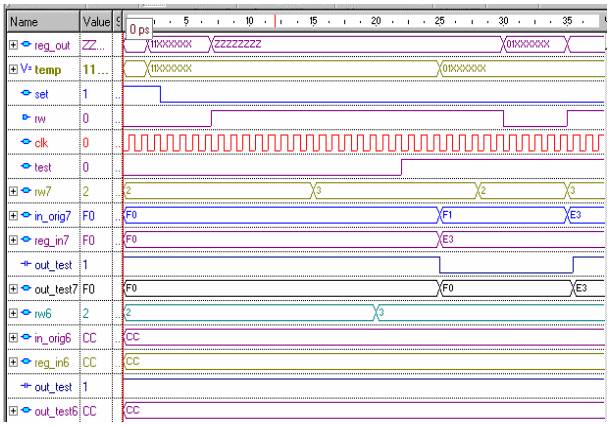

***Figure 8**. Simulation results*

6. CONCLUSION

During the integrated electronic circuit design, testing and diagnostics must be considered as aspects that significantly affect the performances of fabricated chip. Their main influence is reflected in cost-reliability trade. This paper presents one original practical solution of realizing testing-diagnostics functions in the DSP chain of an integrated energy meter. Advantages of the purposed solution are explained. Further improvements of this method are expected in the test logic control and optimal test vectors selection.

REFERENCES

[1] V. Litovski, "Electronic circuit design (in Serbian)", DGIP "Nova Jugoslavija" – Vranje Niš, Yugoslavia, 2000.

[2] Abramovici, M., Breuer, M., and Frideman, A.D., "Digital system testing and testable design", Computer Science Press, New York, 1990.

[3] D. Maksimović, M. Sokolović "Boundary-scan electronic circuit design (in Serbian)", Proceedings for the XLVI conference of ETRAN, Banja Vrućica, Bosnia and Hercegovnina, June 2002. pp. 82 I-85 I.

[4] M. Sokolović, P. Petković "Design for testability in an application specific DSP (in Serbian)", XLVII conference of ETRAN, Herceg Novi, Serbia and Montenegro, June 2003.

[5] ----- "CS5460A Single Phase Bi-Directional Power/Energy IC", CRYSTAL, www.cirrus.com.

[6] Active-HDL, ver. 5.1., ALDEC Inc., 2002.