DESIGN OF HILBERT TRANSFORMER FOR SOLID-STATE ENERGY METER

Bojan Andelković, Milunka Damnjanović, Faculty of Electronic Engineering Niš

Abstract – The measurement of reactive power is gaining interest in modern energy meter chips. In order to calculate reactive power it is necessary to shift phase of voltage signal for 90° relative to current. Hilbert transformer is a digital filter that can be used for this purpose. The filter design procedure and its hardware implementation are presented in this paper.

1. INTRODUCTION

Modern electrical devices besides resistive introduce reactive non-linear loads into power lines so the active energy no longer represents the total energy delivered to customers [1]. Therefore, the measurement of reactive energy becomes very important for energy distributors. In order to calculate reactive power, a dedicated DSP block of an energy meter has to perform the Hilbert transform to get a constant phase shift of 90°.

Hilbert transformer described in this paper is a part of solid-state electrical energy meter. DSP block in this chip has two inputs for the current and voltage signals. The filter should introduce a constant phase shift of 90° in voltage signal while keeping amplitude response as flat as possible. In that way appropriate signal for reactive power calculation is generated.

The filter design algorithm and coefficients optimisation process are described at the beginning. After that, hardware implementation of filter basic building blocks and the complete filter architecture is presented. Synthesis, placement and routing procedures used for circuit layout generation are given in more detail.

2. FILTER DESIGN ALGORITHM

In order to simplify hardware implementation and achieve savings in power consumption, the filter is designed with hardwired coefficients. Therefore the coefficients optimisation process is based on their determining in the form of power of two or canonical signed digit (CSD) with reduced number of non-zero digits [2].

There is a number of advantages provided by CSD code over the ordinary binary representation. Since there are no adjacent nonzero digits in CSD code, less nonzero digits than in the binary representation can be expected. Also, CSD code is expected to be less sensitive to truncation and that can further help in simplifying filter implementation.

Therefore, the following filter design strategy is used:

a) Determine ideal filter coefficients for the target amplitude response using least mean square (LMS) optimisation procedure for linear phase FIR filter design.

b) Convert ideal (infinite precision) coefficients to a set of finite precision integer coefficients

c) For each integer coefficient determine its CSD representation using the algorithm given in [2]

d) Truncate CSD representation by keeping only a specified number of most significant nonzero digits.

Number of filter taps, as well as precision of the coefficients are varied until the desired filter response is achieved. In order to have more efficient hardware implementation number of taps and digits in coefficients are optimised to be as low as possible.

Since flat amplitude response is required only in narrow band around line frequency of 50 Hz, during LMS optimisation process weighting function corresponding to 40 Hz and 60 Hz is set to a large value. Outside of that band weighting function is set to 1.0. However, if we make amplitude response symmetrical around the frequency 0.25fclk, where fclk is filter clock frequency, all odd coefficients in impulse response become zeroes which reduces hardware complexity [3]. Therefore, the same value of weighting function is set for frequencies symmetrical to 40 Hz and 60 Hz around 0.25fclk.

Hilbert transformer is designed according to the following specifications:

- Pass band: 0.5 Hz-2.048 kHz
- Pass band (normalised): 0.000125-0.499875
- Clock frequency: 4.096 kHz
- Symmetry: negative

While optimising filter coefficients the goal was to minimise pass band amplitude response variation in narrow band around 50 Hz. The key features of the designed Hilbert transformer are given in Table 1, while its amplitude response around 50 Hz is shown in Figure 1.

![Fig. 1. Hilbert transformer amplitude response around frequency of 50 Hz (0.0122)](image-url)
Filter coefficients truncated to 4 digit CSD code are generated by the developed C program and given in Table 2. Since amplitude response is symmetrical, all odd coefficients are zeros.

### Table 2.
**Hilbert transformer impulse response coefficients**

<table>
<thead>
<tr>
<th>Coefficient</th>
<th>Value</th>
<th>CSD representation</th>
</tr>
</thead>
<tbody>
<tr>
<td>h(0) = -h(30)</td>
<td>0.710938</td>
<td>1 x ( +1/2^0 -1/2^2 -1/2^5 -1/2^7 )</td>
</tr>
<tr>
<td>h(1) = -h(29)</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>h(2) = -h(28)</td>
<td>0.260742</td>
<td>1 x ( +1/2^2 + 1/2^6 -1/2^8 -1/2^10 )</td>
</tr>
<tr>
<td>h(3) = -h(27)</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>h(4) = -h(26)</td>
<td>0.0488892</td>
<td>1 x ( -1/2^4 + 1/2^6 - 1/2^9 -1/2^14 )</td>
</tr>
<tr>
<td>h(5) = -h(25)</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>h(6) = -h(24)</td>
<td>-0.223145</td>
<td>1 x ( -1/2^2 + 1/2^5 - 1/2^8 - 1/2^11 )</td>
</tr>
<tr>
<td>h(7) = -h(23)</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>h(8) = -h(22)</td>
<td>-0.272461</td>
<td>1 x ( -1/2^2 - 1/2^5 + 1/2^7 +1/2^10 )</td>
</tr>
<tr>
<td>h(9) = -h(21)</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>h(10) = -h(20)</td>
<td>-0.207031</td>
<td>1 x ( -1/2^2 + 1/2^4 -1/2^6 -1/2^8 )</td>
</tr>
<tr>
<td>h(11) = -h(19)</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>h(12) = -h(18)</td>
<td>-0.0189819</td>
<td>1 x ( -1/2^6 -1/2^8 + 1/2^11 +1/2^14 )</td>
</tr>
<tr>
<td>h(13) = -h(17)</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>h(14) = -h(16)</td>
<td>0.554443</td>
<td>1 x ( +1/2^2 + 1/2^4 -1/2^6 -1/2^12 )</td>
</tr>
<tr>
<td>h(15)</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

### 3. HARDWARE IMPLEMENTATION

The general FIR filter architecture can be simplified by exploiting symmetry in Hilbert transformer impulse response. Hardware implementation of symmetrical filter is given in Fig. 2.

Impulse response symmetry is controlled by `symm` signal which can be +1 for positive and -1 for negative symmetry. In this way the number of multipliers is reduced by half. Considering the architecture shown in Fig. 2, two basic building blocks for constructing the filter can be recognised: CSD multiplier and tap adder (Fig. 3).

Having in mind the form of CSD filter coefficients shown in Table 2, the multiplier has to enable multiplication of input signal by every CSD digit and division by its corresponding power-of-two weight. It is constructed with two rows of fulladders and one 16-bit adder at the output. Multiplication by +1/-1 CSD digit is implemented by XOR gates. Specifically, multiplication by -1 is implemented by inverting the multiplicand and setting one of the available LSBs in adder array to logic one. Since this architecture has three LSB positions free but there are four CSD digits, it is necessary to reduce CSD code to have at least one positive digit. Division by power-of-two weight can be implemented by simple bit shifting of the input signal to the right for a specific number of positions. Flip-flop at the output is used for signal synchronization with clock. The adder Σ is implemented as ripple carry adder.

Using the same idea for +1/-1 multiplication, tap adder can be simply implemented as illustrated in Fig. 5.

Using filter basic building blocks it is a straightforward task to map CSD coefficients into the filter architecture shown in Fig. 6. It consists of 8 CSD multipliers (CSDM16x4) and 16 tap adders (TA16). Bit shifting is denoted by "<<" symbols. Delay elements "z⁻¹" are implemented as flip-flops. At the filter output, overflow detection and saturation logic is incorporated. Hilbert transformer contains also clock and reset signals that are not shown in this Figure. In order to compensate for the delay introduced by Hilbert transformer and make quadrature signals, the current signal should be passed through an all-pass filter as shown in Fig. 7.
It can be shown that in order to construct the signal with phase shift of 90° relative to Hilbert transformer output, all-pass filter should be implemented by \((N-1)/2\) flip-flops, where \(N\) equals the number of taps in Hilbert transformer [3].

4. SYNTHESIS, PLACEMENT AND ROUTING

Logic synthesis of VHDL models is performed in program Ambit Build Gates which is a part of Cadence design package [4]. As target technology AMI Semiconductor 0.35um CMOS standard cell library is used. Synthesized Verilog netlist is simulated again and the filter functionality is verified.

After floorplanning, placement and routing in Silicon Ensemble [4], the circuit layout is generated. Also, a clock tree is established.

During this process I/O pins were placed and power rings were constructed. Verilog netlist file generated after this step is again simulated to verify the circuit. The filter was generated as block in order to be incorporated into the complete energy meter chip. Obtained filter area is 865.5 x 967.5um.
5. CONCLUSION

With more and more non-linear reactive loads in electrical devices the reactive power measurement becomes very important for energy distributors.

Hilbert transformer presented in this paper is a part of energy meter chip. It is used to introduce a constant phase shift of 90° in voltage signal. In that way, a quadrature signal necessary to calculate reactive power is generated.

The filter design procedure used for determining impulse response coefficients in CSD form is described. In this way multiplierless filter implementation is possible and some savings in area and power consumption are achieved. Also, the developed filter blocks can be used for realisation of all other digital filters in the chip.

At the moment, a prototype of the energy meter chip is expected and some measurements will be performed to verify the filter VLSI implementation.

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REFERENCES


Sadržaj – Merenje reaktivne snage postaje sve značajnije u savremenim kolima za merenje potrošnje električne energije. Da bi se izračunala reaktivna snaga potrebno je da se signal napona fazno pomeri za 90° u odnosu na struju. Hilbertov transformator je digitalni filter koji može da se koristi u tu svrhu. Procedura za projektovanje filtra i njegova hardverska implementacija opisani su u ovom radu.

PROJEKTOVANJE

HILBERTOVOG TRANSFORMATORA ZA INTEGRISANI MERAČ POTROŠNJE ELEKTRIČNE ENERGIJE

Bojan Andelković, Milunka Damnjanović