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Digital Signal Processing for an Integrated Power-Meter

1 INTRODUCTION

Nowadays, complete hardware and software multi-processor systems are integrated into a single silicon circuit called System-on-Chip. Architectural design is not only about choosing and assembling components together to create a coherent system. It's also making sure that the designed architecture is the right one, capable of successful delivery the system functionality while respecting other constraints such as timing constraints, cost, power consumption, etc. Digital signal processing module (DSP) presented in this paper is a part of an integrated power meter, performing several functions: three-phase energy consumption measuring, providing informations about frequency, current and voltage levels, power and energy consumption. It is a mixed signal system that consists of analog and digital signal processing blocks (Fig. 1). As can be seen in Fig. 1, analog voltage and current signals are processed within appropriate sigma-delta modulators. Then, decimation of sampled signals is performed through the appropriate digital filters. Hilbert digital filter takes output data from voltage decimation filter on it's input, and produces 90 degrees phase-shift signal on it's output. Data rate of current, voltage and phase-shifted voltage digital values, that enter DSP part, is exactly 4.096 kHz.

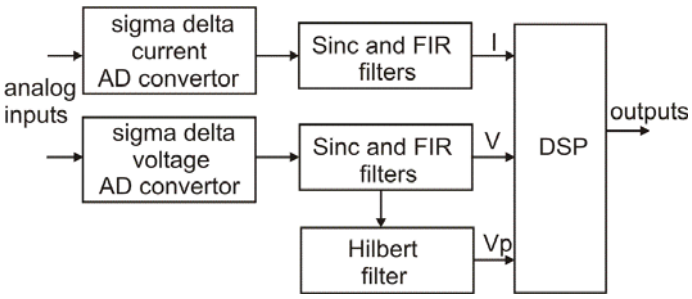


Figure 1. *Main blocks in energy meter IC*

Communication between DSP and external micro controller is done through a serial two-wire interface and allows the user to calibrate various parameters of a meter, including gain, offset and phase errors (in the initialization mode), and read the measured results (in normal operation and testing mode). All registers in the memory are, also, available through the two wire serial interface. DSP is based on controller/datapath partitioning and offers advantages in high-speed operation, low power consumption and significant savings in chip area. Full design procedure from high level system design to synthesis phase, performed by Cadence design system tools, is presented here. The chip is implemented in Alcatel CMOS 0.35μ technology.

2 DSP-MODULE FUNCTION

Based on instantaneous values of current and voltage, DSP performes effective value of current (Ieff), effective value of voltage (Veff), active power (P), reactive power (Q), apparent power (S), and power-factor cos(φ) in every second. It determines the instantaneous value of the power-network frequency with accuracy of 0.01 Hz. Based on calculated values of P and Q, Whr (Wat-hour) pulses are generated for every Whr of the received active and reactive energy. That pulses increment the content of the related registers keeping the values of positive and negative active energy, and positive and negative reactive energy. A short survey of used algorithms would be as follows.

Instantaneous value of current as function of time can be represented in the form:

$$i(t) = \sqrt{2} Ieff \cos(2\pi ft + \varphi) \quad (1)$$

After the discretisation in time, it becomes:

$$i(nT) = \sqrt{2} Ieff \cos(2\pi \frac{f}{f_{sempl}} n + \varphi) \quad (2)$$

where f = 50Hz, f_{sempl} = 4096 Hz.

Effective value of current, Ieff, is calculated once per second according to the expression:

$$Ieff = \sqrt{\frac{\sum_{n=1}^{N} i(nT)^2}{N}} \quad (3)$$

where N=4096. Relative error of the Ieff-calculation is the function of power-network frequency. Similar expression, like for Ieff, is used for Veff calculation. The same stands for relative error.

The relation

$$S^2 = P^2 + Q^2 \quad \textbf{(4)}$$

between apparent power (S), active power (P) and reactive power (Q), suggest us that it is enough to calculate two of three values and then use (4) to find the third. If the instantaneous values of current and voltage are as follows,

$$i(t) = \sqrt{2} Ieff \cos(2\pi ft + \varphi 1) \quad (5)$$

$$v(t) = \sqrt{2} Veff \cos(2\pi ft + \varphi 2) \quad (6)$$

the *instantaneous power* is

$$p(t) = i(t) * v(t) \quad (7)$$

After the discretization of the instantaneous power, the *active power* is calculated according to:

$$P = \frac{\sum_{n=1}^{N} p(nT)}{N} \quad (8)$$

Possible sources of error in active power calculation are the phase difference between voltage and current values and the fact that power-network frequency is slightly changed around the nominal (50Hz), so there is not an integer number of voltage half-periods in a second.

Apparent power and *power-factor Cos(φ)* are calculated according to (9) and (10):

$$S = Ieff * Veff \quad (9)$$

$$\cos(\varphi) = P / S \quad (10)$$

Error eliminating is necessary, so after the multipication of the current and voltage values, the values $i^2(t)$, $u^2(t)$, p(t) i q(t) are filtered, accumulated 4096 times per second and the achieved total is devided with 4096 every second.

3 DSP-MODULE ARCHITECTURE

DSP module has four working modes: reset, initialization, normal operation and testing mode. In the normal operation mode, with the accuracy less than 0.1%, it calculates root mean square values for voltage and current, mean values for active and reactive power, apparent power, active and reactive energy, power factor and frequency. The current input dynamic range is from 10 mA RMS to 100 A RMS, and voltage is up to 300V RMS. It's base clocking frequency is 4.194 MHz.

DSP consists of several blocks: controller, static single port 64x24 bit Random Access Memory, four working registers, arithmetical units for addition, subtraction, division, square-rooting, multiplication and other digital blocks. Digital blocks are divided into several main groups shown in Fig. 2. There is a single 24-bit data bus connecting working registers of DSP to memory block. The control path of DSP unit (controller) is implemented as a finite state machine and it generates a number of control signals that determine what component can write to bus, what registers are loaded from the bus and what arithmetical operation is performed. In normal operating mode, controller performs the periodically repeated sequence that lasts exactly 1024 clock periods. It is divided into four subsequences. Each subsequence lasts exactly 256 clock periods (Fig. 3). The first three controller's subsequences are called R, S and T and they control the calculations made for each phase of the three-phase energy system. At the beginning of each subsequence R, 24 bit instantaneous waveform samples of current; voltage and phase-shifted voltage are transferred from Hilbert and decimation filter outputs into the memory. After that, instantaneous sample of current I is squared in multiplication unit. Multiplier takes 18-bit operands and produces 36-bit result within 18 clock periods. Then, the value I^2 is passed throught the single pole Low Pass Filter (LPF) with a cut-off frequency of 10Hz, and after that, it is accumulated into a 48-bit register $AccI^2$ (Fig. 4a).

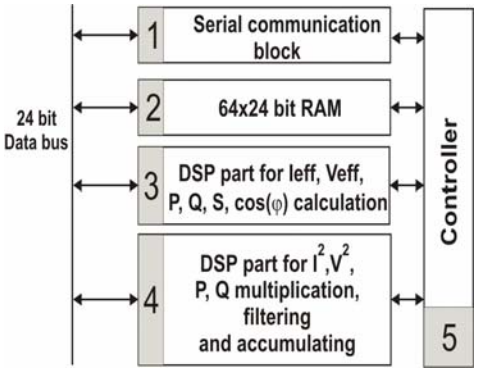


Figure 2. *DSP block diagram*

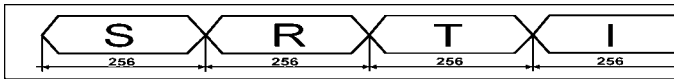
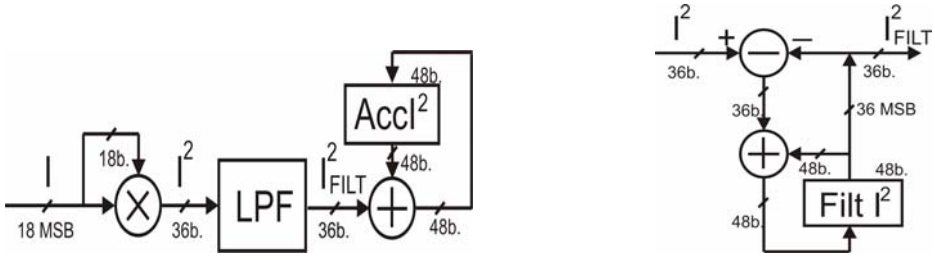


Figure 3. *Controller's subsequences*



(a) *(b)*

Figure 4. *(a) Data processing chain for current-square accumulation*
(b) Low pass filter

Low pass filter helps in reducing the calculation error that could exist due to the fact that time-interval of 1 second (that is, accumulating time for the value I^2) doesn't always happend to be integer number of power-line-signal half-periods. LPF data processing chain is shown in Fig. 4b, and its transfer function is:

$$H(z) = \frac{Y(z)}{X(z)} = \frac{2^{-6}}{1 - z^{-1}(1 - 2^{-6})} \tag{11}$$

Therefore, LPF is easy for implementation. Part of a DSP's hardware in which these operations are done is shown in Fig. 5. The LPF uses registers RegA and RegB and arithmetical addition and subtraction units. The content of 48-bit register $AcclI^2$ (Fig. 4a) and the content of the register $FiltI^2$ (Fig. 4b) are stored in RAM block.

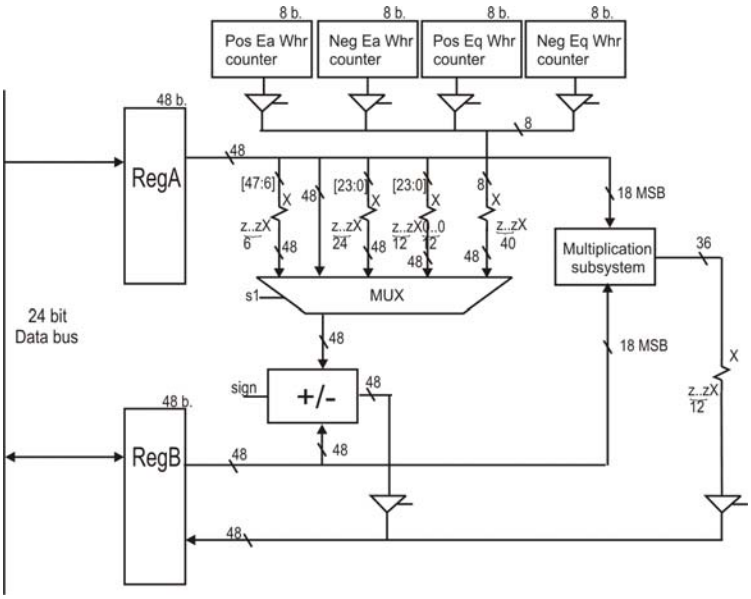


Fig. 5. *Structure of DSP block 4*

The same procedure is performed and the same hardware is used for V^2. Active and reactive power accumulation is done through the same procedure. The only difference is in multiplication process: voltage- and current-samples' values are multiplied for active power accumulation, and current-sample value is multiplied with phase-shifted voltage-sample for reactive power accumulation. The fourth subsequence of the controller, denoted E, manages the calculations that are periodically repeated every second. Based on accumulated squares of instantaneous current and voltage, and accumulated instantaneous active and reactive power during the last second, calculations are performed in order to generate voltage and current root mean square (RMS) and mean active and reactive power values.

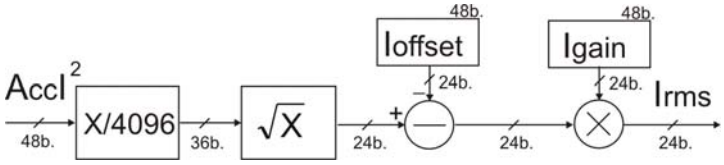


Figure 6: *Data processing chain for current RMS calculation*

Block 3 in Fig. 2 implements all these calculations. It's interior structure is shown in Fig. 7. It consists of two registers named RegC and RegD and arithmetical units that implement square rooting, subtraction, multiplication and division. To generate current root mean square, accumulated sum is stored into RegC and devided by 4096. Next, square rooting operation is performed over the average value of voltage square, current offset is subtracted, multiplied with gain correction and root mean square of current is obtained (Fig.6). The same procedure stands for root mean square of voltage. Mean active and reactive power calculation is similar, except there is no root calculation. Apparent power is obtained by multiplying root mean square of current and voltage, and power factor divi-ding active and apparent power.

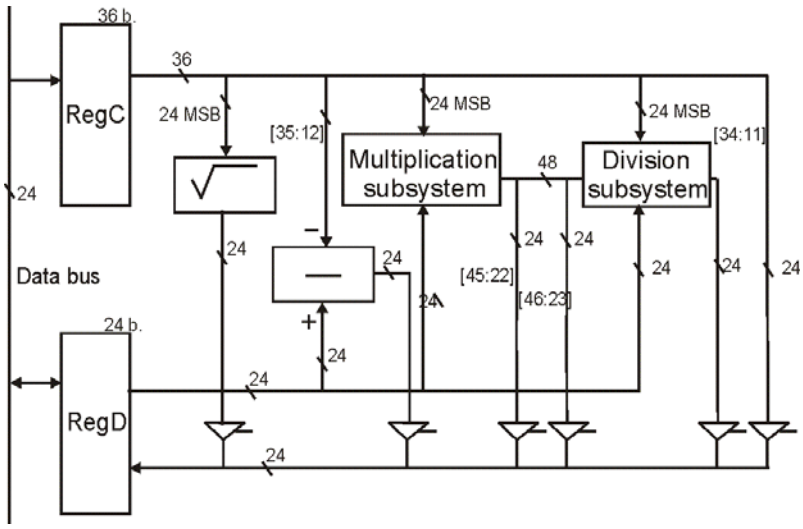


Figure 7. *Structure of DSP block 3*

Instantaneous values of current I, voltage V, phase-shifted voltage Vp, root mean square of current Irms, voltage Vrms, average values active Pav, reactive Qav, and apparent power S, and their offsets Ioffset, Voffset, Poffset, Qoffset are all represented by 24-bit signed two-complement values with a specific data format shown in Fig. 8. Its range is from -1 to 1 and it is normalized to some full-scale value. Full- scale value for the voltage (V, Vp, Vrms, Voffset) is $\sqrt{2}$ 300V, for current (I, Irms, Ioffset) it is $\sqrt{2}$ 100A, for power (Pav, Qav, S, Poffset, Qoffset) it is 2*100A*300V = 60kW.

23	22	21		0
sign	2^{-1}	2^{-2}	...	2^{-22}

Figure 8. *Data format 1*

23	22	21		0
sign	2^{0}	2^{-1}	...	2^{-22}

Figure 9. *Data format 2*

Gain corection values that should be obtained after power meter calibration (Igain, Vgain, Pgain), power factor Cos(φ) and power line frequency F are also represented by 24-bit signed two complement values in range from –2 to 2 and have the data format shown in Fig. 9.

4 DESIGN PROCESS AND SIMULATION RESULTS

To obtain the high level system simulation and verification, an algorithm had been developed and implemented in C. Extensive simulations at high level design enabled us choosing the appropriate data-width and valid ranges of algorithm's variables. Next, the task was to create an architecture well suited to a given algorithm. Techniques inherent pipelining increase throughput of the final design but they come as expense in increased gate number, more difficult implementation of external chip communication and difficult debug later in the design process. Instead, our DSP unit based on controller/datapath partitioning offers advantages in high-speed operation, low power consumption and small area for VLSI implementation.

When architecture was obtained that runs the algorithm efficiently, it was translated into behavioral VHDL description. RTL descriptions were loaded into program for logical synthesis, Cadence's Build Gates that generated the netlist consisting of Alcatel CMOS035 digital library cells. After synthesis, estimated DSP area expressed in logical NAND-gate units, is 10950 units. The extracted netlist was loaded back to Verilog simulator and the simulation was performed using Cadence' NCsim tool with same test bench as before synthesis process and the same results were obtained. Finally, Silicon Ensemble has performed floorplanning, placement and routing, as well as clock and reset trees generation for complete circuit. At the end of logical verification process, Verilog file was extracted from layout and brought back to NCsim simulator where final check of the total digital part of the IC was performed.

5 CONCLUSION

DSP part of power-consumption measuring IC, implemented in 0.35μm CMOS standard cell technology, isdescribed here. Based on controller/datapath partition, fast DSP with low power consumption and small area has been developed. The algorithms and circuitry are described.

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