# DIGITAL SYSTEM FOR POWER LINE FREQUENCY MEASUREMENT

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**Abstract –** *An implementation of power line signal frequency measurement system is considered in this paper. It is a part of energy measurement SoC, aimed for frequencies in range 45 - 65 Hz with accuracy less than 0.02%. The algorithm, entire system realization and functioning is described.*

## 1. INTRODUCTION

Nowadays, complete hardware and software multi-processor systems are integrated into a single silicon circuit called System-on-Chip. Architectural design is not only about choosing and assembling components together to create a coherent system; it's also making sure that the chosen architecture is the right one, capable of successful delivery the system functionality while respecting the other constraints such as timing constraints, costs, power consumption, etc.

Attention has been paid to frequency meter that measures power line signal frequency. It is a part of an energy power meter SoC that beside frequency, calculates other important parameters of power line signal such as effective voltage and current, apparent, active and reactive power, power factor, active and reactive energy. Main optimization criterion for choosing frequency meter was small chip area. Proposed circuit shares a great part of its hardware with the other IC digital blocks having different functions.

Frequency measurement system is considered starting with explanation of measurement procedure. After that, exact hardware implementation is described. System was verified through the VHDL simulations and synthesized by Cadence tools, and the results are presented.

## 2. FREQUENCY MEASUREMENT PROCEDURE

Energy meter IC consists of several main analog and digital parts shown in Figure 1. Analog part has two sigma delta AD converters for current and voltage channels. Digital part consists of digital filters and main DSP block. Namely, after digital Sinc, FIR and Hilbert filters, 24 bit sign two's complement digital samples of current, voltage and phase shifted voltage are produced and come to DSP block inputs I, V, Vp (Fig. 1). These voltage and current samples change their values with clock frequency of 4096Hz.

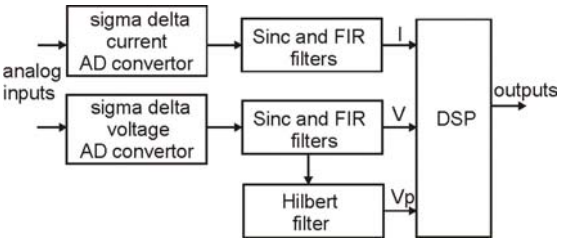


Figure 1. *Energy Power Meter System-on-Chip*

DSP block (Fig. 2) gets samples of voltage, current and phase shifted voltage, and calculates following power line parameters: current and voltage RMS values, apparent S, active P and reactive Q power, power factor Cos(φ), frequency f, reactive Eq and active Ea energy. The controller, main part of DSP, manages all other parts of DSP including frequency measurement circuit.

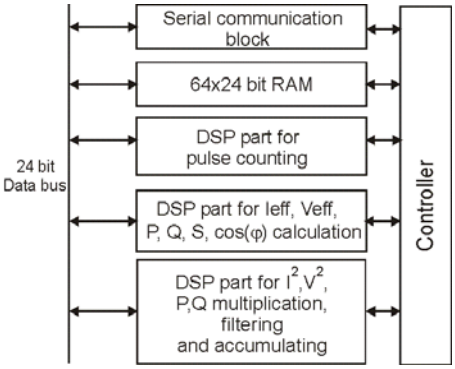


Figure 2. *Parts of DSP*

The most significant bit of voltage samples determines the voltage sign and, therefore, the period of power line signal. Therefore, voltage sign signal can be used for frequency measurements. The main idea is as follows.

During the measurement interval of 100 periods of the voltage sign signal, that will be referred as *time base* in the rest of paper, counting circuitry count pulses generated by controller. These, so called *counter pulses* have constant frequency $f_{sample}$=4096Hz controlled with an off-chip quartz oscilator. Counting starts when *counting-start* signal is asserted (by the controller) and voltage sign signal crosses zero. The voltage samples, voltage sign, counting-start, time base and counting pulses are shown in Fig. 3.

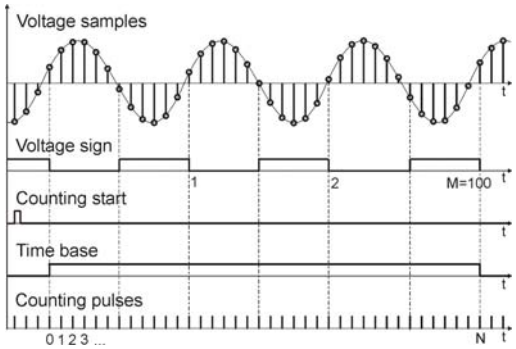


Figure 3. *Signals relevant for frequency measurement*

Actually, two counters are needed. The first one counts the voltage sign periods and the other counts counter-pulses. These short pulses, generated by the controller, are synchronized with the voltage samples (Fig. 3). After 100 periods are encountered, time base is over and the counter stops. It is important to note that number of counted pulses is proportional to the time base duration.

Power line frequency doesn't change abruptly, so it is sufficient to measure a new frequency value after every

fourth second. Therefore, frequency is calculated as an average obtained after exactly 100 periods of 50 Hz power line signal. Afterward, the controller generates new start signal that starts the next counting sequence.

The calculated frequency value is represented by 24-bit two's complement value as normalized value (like all other results in DSP) relative to frequency of 50 Hz.

The sign of digital voltage samples is determined by voltage signal cross through the zero. If shorter time of frequency computation is demanded, other methods should be used which include analog comparator. In our case, that was not necessary: proposed circuit satisfies the requirements about measuring frequency in range 45 Hz to 65 Hz with accuracy less than 0.02 %. Two worst cases with the greatest relative errors are shown in Fig. 4.

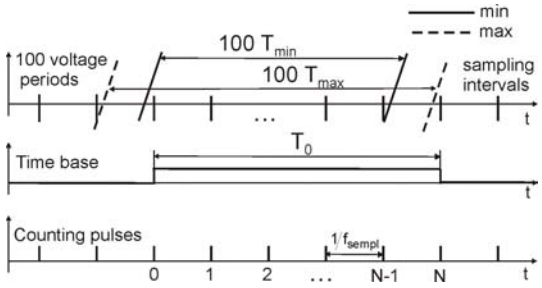


Figure 4. *Maximum and minimum durations of 100 power voltage periods relative to sampling intervals*

The number of counted pulses, N, is determined by the duration of time base interval and $f_{sample}$. Thus,

$$N = T_0 * f_{sample}\ , \tag{1}$$

where $f_{sample}$ = 4096Hz.

The maximum worst case occures when line voltage leads at the begining of the measured interval and lags at the end, referred to the ideal case (Fig. 4). Then interval of 100 voltage periods is measured as:

$$T_{max} = (N+1)/f_{sample}\ . \tag{2}$$

The minimum worst case occures when line voltage lags at the begining and leads at the end of the measured interval, respectively to the ideal case. Then the time interval of 100 periods is:

$$T_{min} = (N-1)/f_{sample} \tag{3}$$

Therefore, in both worst cases, error is only one pulse.

### 3. PULSE COUNTING CIRCUIT

Ports of the proposed pulse counting circuit are given in Fig 5. Input signal *ld_V* is generated by the control unit. Its frequency is 4096 Hz and duration is 1024 times shorter than its period. The voltage sample from main DSP bus, *Data(23:0)*, is stored on its rising edge into appropriate RAM memory location.

Input signals *Reset*, *Pulse*, *Start_FM* and *Oe* are generated by the control unit that operates at working frequency $f_{clk}$ = 4096x1024 Hz. All these pulses have very short duration, equal to a reciprocal value of control unit frequency. Input signal *Reset* raised after start up initializes

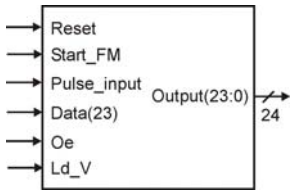


Figure 5. *Pulse-counting circuitry interface*

counters to zero. Signal *Pulse* is the pulse-sequence of frequency of 4096 Hz being counted inside the circuit. *Start_FM* represents the counting start signal. It is asserted once after every four seconds and initializes counters to zero, as well. Signal *Oe* is output enable signal. When it is active, the number of counted pulses is put on the main bus *data(23:0)* for further processing.

Internal structure of the Pulse-counting circuit is shown in Figure 6. It consists of two counters. Counter 1 counts periods of voltage signal. Whenever *time_base* signal is active, counter 1 counts rising edges of the *sign* signal that represents the voltage sign. Voltage sign is derived from the most significant bit of the bus (*Data(23)*) into a D flip-flop (Fig. 6). The counter stops when hundred pulses are encountered. It means that *time_base* signal is stated on the second D flip flop output. When it rises to logic one, circuit starts counting (Fig. 4).

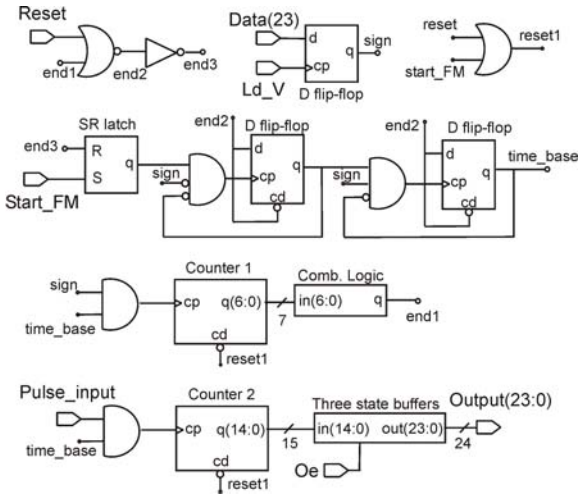


Figure 6. *Internal structure of counting circuitry*

Counter 2 is triggered by counting pulses represented as Pulse_input signal in Fig. 6. The output is 15-bit bus. When signal *time_base* is active, circuit counts rising edges of signal *Pulse_input.* When time base become inactive, counting is desabled. Value that remains in Counter 2 is the number of pulses for time interval of 100 power line periods.

Circuit-inside control logic provides that after start-counting signal is asserted, circuit starts counting when most significant bit of voltage becomes logic 1. Signal *Start_FM* (Fig. 6) sets SR latch and resets counters 1 and 2. Also signals *end1, end2* and *end3* become inactive and circuit is ready for new counting.

### 4. DIVISION CIRCUIT

The division circuit is used in frequency and power factor, Cos(φ), calculation. Dividend and divisor are

represented by 24-bit signed two's-complement values with the same format. Dividend can be positive or negative but divisor is always positive. Quotient is also 24-bit two's-complement number with the format shown in Fig. 7. It is rational number in range from –2 to 2. Decimal point is after second most significant bit. Division is obtained in exactly 24 clock periods.

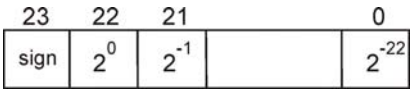


Figure 7. *Data format*

Division circuit is shown in Fig. 8 and consists of three registers called U0, U1 and U2, a unit for addition and subtraction U3 and control unit U4. Register U1 has 25 bits. U0 and U2 have 24 bits. Arithmetic unit U3 has ripple architecture.

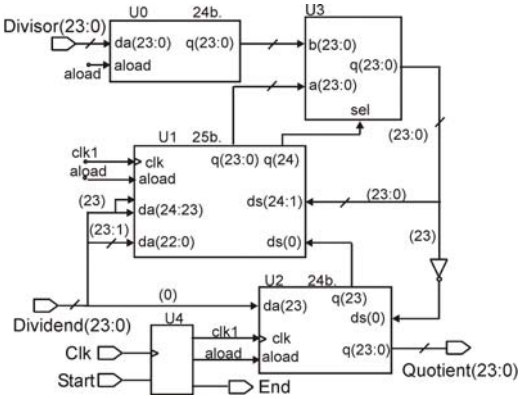


Figure 8. *Internal structure of division system*

At the operation beginning, dividend has to be stored into registers U1 and U2. Higher 23 bits of dividend are stored in lower 23 bit positions of register U1. The sign of dividend is stored in two most significant bit positions of U1 and the lowest dividend bit is stored in most significant bit of U2. The other bits of U2 are reset to zero. Divisor is stored in 24-bit register U0.

After every clock period, subtraction or addition is performed and results are stored into registers. The most significant bit of U1 determines whether subtraction or addition is to be performed. If it is zero, subtraction of numbers U1(23:0) and U0(23:0) is performed. Result is stored in U1(24:1) and U2 is shifted one bit left. Previous most significant bit of U2 is stored in the least significant bit of U1. The inverted sign of the derived subtraction result is stored in the least significant bit of U2.

$$\begin{aligned} &U1(24:1) := U1(23:0) - U0(23:0) \\ &U1(0) := U2(23) \\ &U2(23:1) := U2(22:0) \\ &U2(0) := (U1(23:0) - U0(23:0)) > 0 \end{aligned} \tag{4}$$

If the most significant bit of U1 is one, addition of numbers U1(23:0) and U0(23:0) is performed. Result is stored in U1(24:1) and U2 is shifted one bit left. Previous most significant bit of U2 is stored in the least significant bit of U1. The inverted sign of the derived sum is stored in the least significant bit of U2:

$$\begin{aligned} &U1(24:1) := U1(23:0) + U0(23:0) \\ &U1(0) := U2(23) \\ &U2(23:1) := U2(22:0) \\ &U2(0) := (U1(23:0) + U0(23:0)) > 0 \end{aligned} \tag{5}$$

Operation is finished after 24 clock periods. After 24 clock periods, the quotient remains in register U2.

## 5. FREQUENCY CALCULATION CIRCUIT

A part of DSP, used for frequency calculation, is shown in Fig. 9. Beside frequency, DSP calculates other values such as effective current and voltage, active, reactive and apparent power and power factor. It consists of two registers (named RegC and RegD) and several arithmetical units: square rooting, division, multiplication, and subtraction unit.

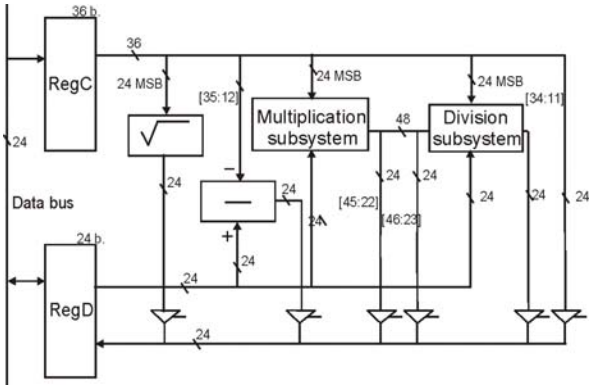


Figure 9. *Block of Ieff, Veff, P, Q, S, cos(φ) and Frequency calculation*

For the frequency calculation, there is a register in RAM memory, that saves the number of pulses for exactly 100 periods of 50 Hz power line signal, stored during the initialization mode of chip. Whenever frequency is to be calculated, this register is read and value stored into register RegC. It represents the dividend. The divisor is the number of counted pulses, which is read from circuit described in section 3, and stored into register RegD.

Division operation is executing once after every four seconds. After asserting start signal for division by the controller, previously described sub-circuit for division generates the quotient. It is stored into RegD and back to the memory into the memory location reserved to save the measured frequency.

After that, start signal for pulse counting is asserted and frequency measurement operation is repeated.

The frequency is represented by 24-bit value, normalized relative to 50Hz, and its format is given in Fig. 7.

## 6. SIMULATION AND SYNTHESIS RESULTS

Circuit described in VHDL was first verified with VHDL simulator Active HDL. The testbenches for pulse counting circuit, division subsystem and whole DSP were written and appropriate input stimuli and clock signal defined.

Results based on test bench for impulse counting circuit, are counter's outputs. For 100 periods of 50 Hz signal, 100 periods and 8192 impulses were counted.

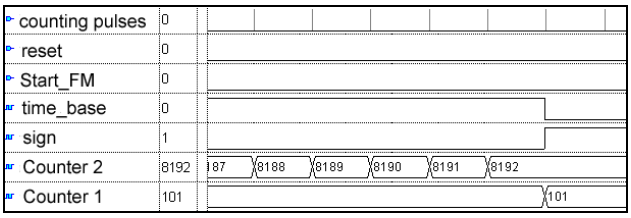


Figure 10: *Simulation results*

Result of simulation based on division circuit test bench is derived quotient. In the proposed example shown in Figures 11 and 12, dividend and divisor are the same numbers (002000)h. The result, hexadecimal number (400000)h, is obtained after 24 clock cycles.

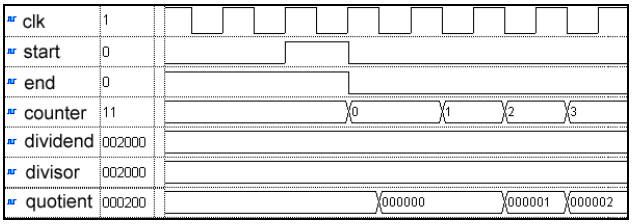


Figure 11: *Simulation results*

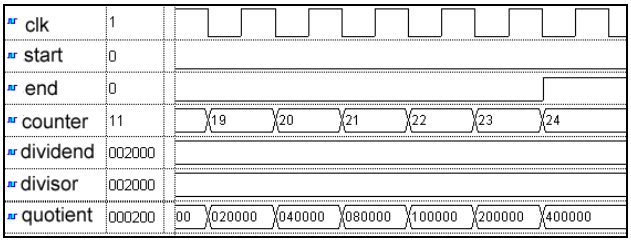


Figure 12: *Simulation results*

For whole DSP, testbench results represent all power line parameters. Frequency value is just one of them.

After, VHDL descriptions were loaded into program for logical synthesis, Build Gates (Cadence design system part, [4]). Build Gates generated netlist consisting of Alcatel 0.35μm CMOS digital library cells. The estimated areas for pulse counting circuit, division system and DSP after completed synthesis processes, expressed in logical NAND gates and square millimeter units, are given in Table 1.

*Table 1.*

| System / Area units | Pulse counting circuit | Division system | DSP |
|---|---|---|---|
| NAND gate | 285 | 593 | 11437 |
| $mm^2$ | 0.0319 | 0.0664 | 1.28 |

Standard cells' netlist for whole DSP was extracted during the synthesis process, and loaded back to VHDL simulator in a form of Verilog file. This time, the simulation was performed using NCsim logical verification tool from Cadence package applying the same testbench as used for synthesis process. Obtained results were unchanged. Design verification process was completed successfully.

The frequency measurement circuit was built in the rest of circuitry, and floor planning, placement and routing were performed using Cadence' program Silicon Ensemble, as well as clock and reset trees generation. At the end, Verilog file was extracted and brought back to NCsim simulator where final check of the total digital part of the IC was performed. Finally, layouts were verified by Design Rule Check analysis.

## 7. CONCLUSION

The proposed frequency measurement system is a part of DSP block in electrical power measurement IC. It has two main blocks - pulse-counting and division subsystem. The division operation circuitry is shared with other functional blocks of DSP. In fact, only counter subsystem, i.e. only small area, has been added to DSP to accomplish the function of frequency measuring. Therefore, DSP occupies as small area as possible.

The result of frequency measuring is compatible with other results that DSP provides. It is rational number represented by 24 bits long value, in range from 0 to 2, relative to value of 50 Hz.

System is capable for measuring the frequencies from 25 Hz to 100 Hz. Frequency of 50 Hz can be measured with accuracy of 0.0122 %, 60 Hz with 0.0146 % and signal of 100 Hz with 0.0244 % accuracy.

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**Sadržaj** – U radu je razmotrena implementacija kola za merenje frekvencije koje je deo složenog sistema na čipu za merenje potrošnje električne energije. Kolo meri frekvencije od 45 do 65 Hz sa tačnošću boljom od 0.02 %. Kompletno je opisan način rada i prikazani rezultati simulacije i fizička realizacija sistema.

**DIGITALNI SISTEM ZA MERENJE FREKVENCIJE MREŽE**

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