Single-phase power/energy meter IC

Features

- **Energy data accuracy: Meets IEC 1036 (classes 1 and 2) and IEC 687 (classes 0,2 S and 0,5 S)**
- **On-chip functions: Active, Reactive and Apparent Power and Energy Measurement, Power Factor, Frequency, I_{RMS} and V_{RMS}, energy to pulse-rate conversion**
- **On-chip bandgap reference 1.205 V**
- **Calibration of Gain and Phase Error**
- **Measurement Bandwidth of 1800Hz**
- **Built-in self test**
- **Simple three wire serial interface**
- **Power supply $V_A=V_D=3.3$ V**
- **Dynamic range of 10000:1 in current and more than 1000:1 in voltage channel**

Description

LEDA 08 (IMPEG01) is highly integrated CMOS power meter IC. It is designed to accurately measure and calculate: active reactive and apparent power and energy, power factor, I_{RMS}, V_{RMS} and frequency for 2 or 3 wire power meter applications.

Basically, it comprise two $\Delta\Sigma$ Analog-to-Digital Converters (ADC), digital decimation filters, DSP dedicated for high speed power calculation functions and a serial interface on a single chip.

The LEDA 08 (IMPEG01) interfaces to low-cost off-chip components to measure current and voltage. Simple shunt resistor or transformer is suitable to convert current into input voltage for the current channel, and resistive divider or potential transformer are appropriate to adjust line voltage for the input to the voltage channel. The LEDA 08 (IMPEG01) features a bi-directional serial interface for communication with a micro-controller and a programmable frequency output that is proportional to energy. AC system-level calibration allows offset and gain correction for current, voltage and power.

The "Auto-Boot" feature allows 'stand-alone' function and self-initialization on system power up. In Auto-Boot Mode, the LEDA08 (IMPEG01) reads the calibration data and start-up instructions from an external EEPROM. In this mode, the LEDA08 (IMPEG01) can work without the need for a microprocessor, for low-cost metering applications.

ORDERING INFORMATION:

N/A

1. GENERAL DESCRIPTION

Figure 1 shows the structure of LEDA08 (IMPEG01). The LEDA08 (IMPEG01) is designed for power measurement applications and is optimized to interface to a shunt or current transformer to measure current, and a resistive divider or transformer to measure voltage. With single +3.3 V supply on both of the input channels accommodate common mode + signal levels between -0.25 V and VA+. Recommended input voltage swing is ±125mV.

The LEDA08 (IMPEG01) includes two high-rate digital decimation filters, which reduce output word rate of signals obtained in ΣΔ ADC from 524288Hz to 4096Hz. These filters yield 24-bit output data word.

To facilitate communication to a microcontroller, the LEDA08 (IMPEG01) includes a simple three-wire Communication Serial Port (CSP) interface. The serial port has Schmitt Trigger in its SCLK (serial clock) pin to allow for slow rise time signals.

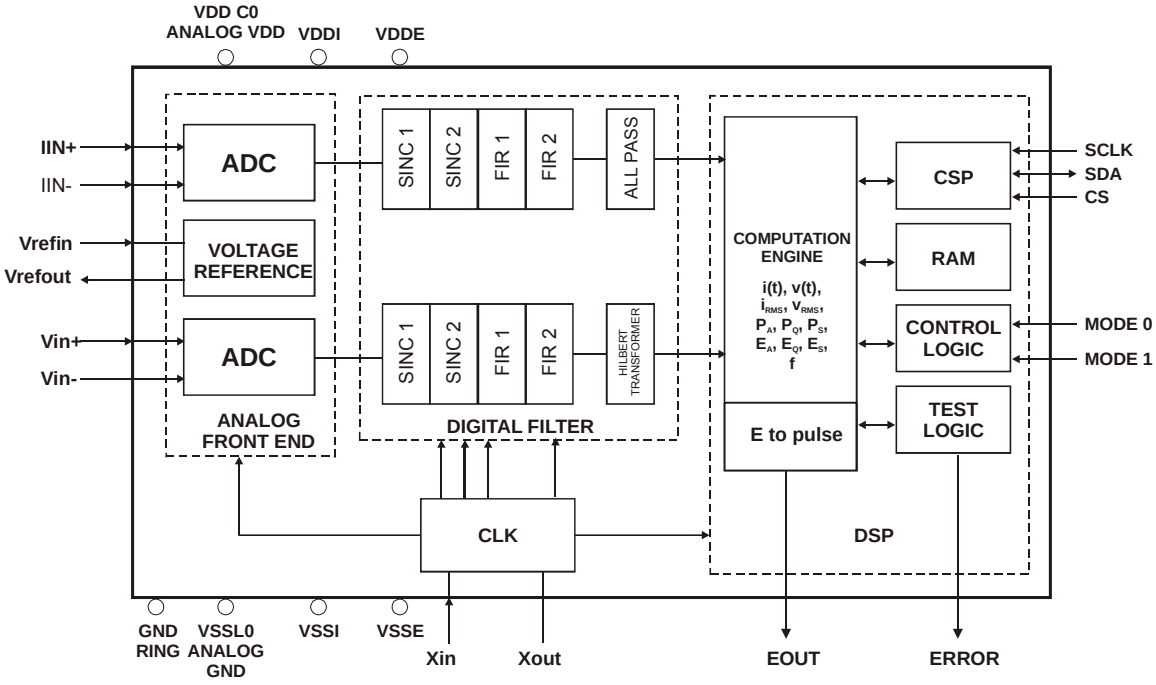

Figure 1 Block diagram of LEDA 08 (IMPEG01)

2. THEORY OF OPERATION

A computational flow diagram for the two data paths is shown in Fig. 2.

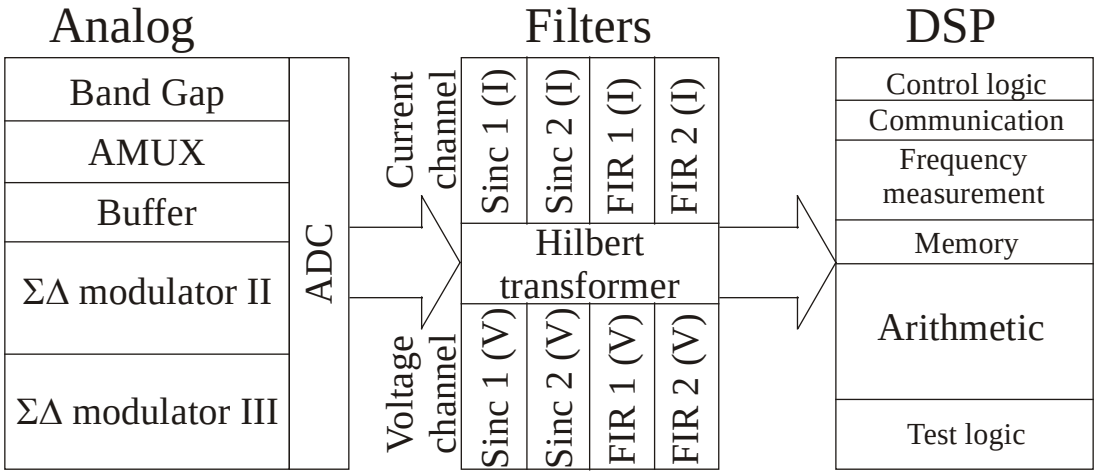

Figure 2 Dataflow in LEDA 08

2.1 Input stages

Two pairs of input analog signals enter as voltage signal ranged 0-250mV pick-to-pick. One input pair corresponds to the voltage channel (pins VIN+ and VIN-) while voltage equivalent of current enters into the current channel through pins IIN+ and IIN-. Analog signals are converted into digital using ΔΣ oversampling modulation technique. The dynamic of 10000:1 in the current channel provides a third order ΔΣ modulator realized as 2-1 MASH structure. The 2-1 architecture is preferable to alternative cascaded third-order architectures because it is less sensitive to component mismatch. The architecture is implemented by combining three summing integrators with two comparators and two single-bit D/A converters. The second order ΔΣ modulator in voltage channel gives dynamic range better than 100:1. Modulators are realized as fully differential with correlated double sampling first integrator. There is internal bandgap voltage reference that is accessible through VREFOUT pin or can be replaced by external reference through VREFIN pin. The circuit provides referent voltage of 1.205 V at 27 °C with temperature coefficient of 6 ppm/°C. Analog multiplexer denoted as AMUX in Figure 2 enables access to particular test points within the analog part.

2.2 Digital filtering

Analog signals sampled with rate of 524288 Hz are downsampled to 4096 Hz. Decimation factor of 128 is realized as a four-stage 8-4-2-2 decimation filter. Each decimator consists of 4 blocks, as shown in Figure 3.

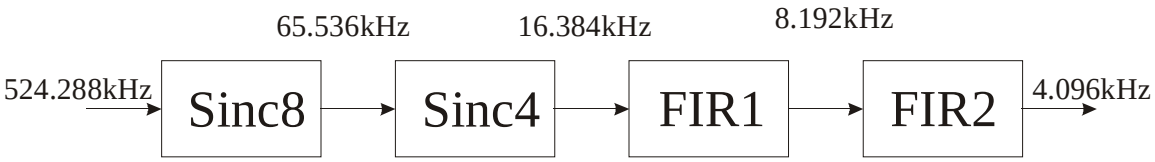

Figure 3 Decimation filter chain in LEDA 08

Simultaneously, the filter section removes HF noise. There are 2 Sinc filters and 2 FIR filters. The first stage has a heavy impact on the total number of digital filter operations. The Sinc filter is chosen for the first and the second stages because it can be conveniently implemented in a very efficient manner. Furthermore, in the first stages the antialiasing requirements are highly relaxed. The slight distortion of amplitude characteristics introduced by Sinc architecture is equalized in the following stages of the decimator, with almost negligible cost. The successive two filters are halfband FIR filters in both channels.

Hilbert transformer applied to the voltage signal enables utilization of the same hardware for active and reactive power calculation. Simultaneously, in order to keep the same delay in both channels, the all-pass filter is employed in the current channel, as Figure 1 shows.

2.3 DSP

DSP consists of serial communication block, static single port 64x24 bit Random Access Memory, Computation Engine divided in two parts, and Controller block, as indicated in Figure 4. 24-bit Data bus connects working registers with RAM memory. Controller manage DSP operation.

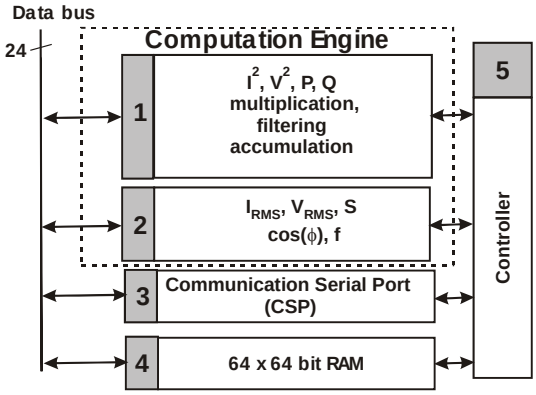

Figure 4. Structure of DSP block

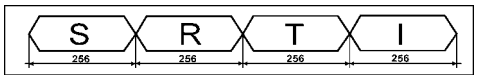

Figure 5. Timing of Controller subsequences

Although LEDA08 (IMPEG01) is dedicated for single phase power measurements the Controller is designed for three-phase application. It is implemented as a finite state machine and it generates all control signals responsible to determine what data can be written to bus, what registers should be loaded from the bus and what arithmetical operation is going to be performed. During the normal operating mode, controller performs periodically repeated sequence that lasts exactly 1024 clock periods. It is divided in four subsequences of exactly 256 clock periods according to Figure 5. The first three subsequences denoted by R, S and T control the calculations made for each phase of the three-phase energy system. The last subsequence, I, is reserved for computations regarding the overall power consumption and the self-testing procedure.

DSP operates in four modes defined by digital signals on pins MODE1 and MODE0 as given in Table 1.

Table 1 ***Operation mode control***

pin name/ mode	normal	initialization	test	reset
MODE1	0	0	1	1
MODE0	0	1	0	1

2.3.1 Computation Engine

The Computation Engine (CE) calculates I_{RMS}, V_{RMS}, active (P) reactive (Q) and apparent power (S) and energy (E_P, E_Q, E_S, respectively), power factor ($\cos\varphi$) and frequency (f) using measured values of instantaneous current (i(t)) and voltage (v(t)) as input data. Actually, as indicated in section 2.2, except v(t) the $\pi/4$ phase shifted value of v(t) is used to launch CE, as well.
Additional block transforms energy into pulses providing one pulse for every Whr of measured active and reactive energy. That pulses increment the content of the related registers keeping the values of positive and negative active energy, and positive and negative reactive energy. This section gives a short survey of used algorithms.
Instantaneous value of current can be represented in the form:

$$i(t) = \sqrt{2} I_{rms} \cos(2\pi f t + \varphi). \quad (1)$$

After the discretisation, it becomes:

$$i(nT) = \sqrt{2} I_{rms} \cos(2\pi f nT + \varphi) = \sqrt{2} I_{rms} \cos(2\pi n \frac{f}{f_{semp}} + \varphi), \quad (2)$$

where f = 50Hz,T=1/f_{semp} = 1/4096 Hz.

I_{rms}, is calculated once per second according to the expression:

$$I_{rms} = \sqrt{\frac{\sum_{n=1}^{N} i(nT)^2}{N}} \quad (3)$$

where N=4096. Similar expression is used for V_{rms} calculation.
The relation (4) connects apparent power (S) with active (P) and reactive power (Q):

$$S^2 = P^2 + Q^2. \quad (4)$$

It suggest that it is sufficient to calculate two of three values and then use (4) to find the third.
Basic for active power calculations are instantaneous values of current and voltage that can be assumed as:

$$i(nT) = \sqrt{2} I_{rms} \cos(2\pi n \frac{f}{f_{sep}} + \varphi 1)$$
$$v(nT) = \sqrt{2} V_{rms} \cos(2\pi n \frac{f}{f_{sep}} + \varphi 2) \quad (5)$$

The *instantaneous power* is

$$p(nT) = i(nT) \cdot v(nT), \quad (6)$$

and the *active power* is calculated according to:

$$P = \frac{\sum_{n=1}^{N} (i(nT) \cdot v(nT))}{N} \quad (7)$$

Apparent power and *power-factor Cos(φ)* are calculated according to (9) and (10):

$$S = I_{rms} \cdot V_{rms}; \quad (9)$$

$$\cos\varphi = \frac{P}{S}. \quad (10)$$

As power is calculated in interval of one second, the conversion to energy is straightforward.

In order to minimize error after the multiplication, the values $i^2(t)$, $v^2(t)$, p(t) i q(t) are filtered, averaging for one second after 4096 samples.

DSP module operates in four working modes: reset, initialization, normal operation and testing mode.

2.3.2 Computation Engine Architecture

At the beginning of each single-phase subsequence (S,R and T), the samples of current, voltage and phase-shifted voltage are transferred from filters into the memory in a form of 24 bit data. Then, hardware presented in Figure 6 calculates the value I^2. Low pass filter helps in reducing the calculation error due to inconsistency of clock frequency. The values accumulated for one second is accumulated into a 48-bit register $AccI^2$.

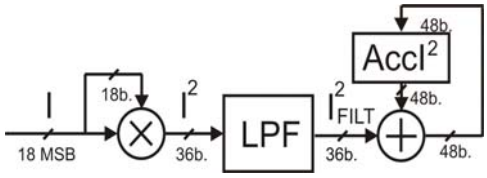

Figure 6. Data processing chain for current-square accumulation

The same procedure and the same hardware is used to calculate V^2 and active and reactive power. The only difference in power calculation stands for multiplicands where current samples are multiplied with voltage or with phase-shifted voltage samples in order to obtain instantaneous active and reactive power, respectively .

Subsequence denoted as I in Figure 5, manages the calculations that are periodically repeated every second. Calculations related to I_{rms}, V_{rms} and mean active and reactive power are based on accumulated squares of instantaneous current and voltage, and accumulated instantaneous active and reactive power during the time interval of one second.

Figure 7 shows hardware implementation of CE part dedicated for root mean square calculation.

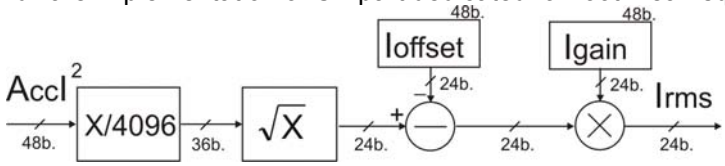

Figure 7: *Data processing chain for current RMS calculation*

The accumulated sum of 4096 samples I^2 is divided by 4096 and square rooting operation is performed. Thereafter the corrections for current offset and gain may be imposed. The same procedure stands for root mean square of voltage. Mean active and reactive power calculation is similar, except there is no root calculation. Apparent power is obtained by multiplying root mean

square of current and voltage and dividing active with apparent power gives power factor.

Instantaneous values of current I, voltage V, phase-shifted voltage Vp, Irms, Vrms, average active Pav, reactive Qav, and apparent power S, and their offsets Ioffset, Voffset, Poffset, Qoffset are all represented by 24-bit signed two's-complement values in the specific data format shown in Fig. 8. This format ranges from -1 to 1 and it is normalized to the specific full-scale (FS) value given in Table 2.

Table 2 ***Full-Scale Ranges***

	Current	**Voltage**	**Power**
Range (FS)	$\sqrt{2}$ 100A	$\sqrt{2}$ 300V	60kW
Max Input	±125mV	±125mV	not applicable

Gain calibration values (Igain, Vgain, Pgain), power factor Cos(φ) and power line frequency F are represented by 24-bit signed two's complement values ranged from –2 to 2 in data format shown in Fig. 9.

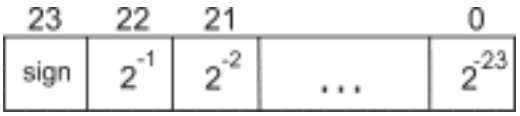

Figure 8. *Data format 1*

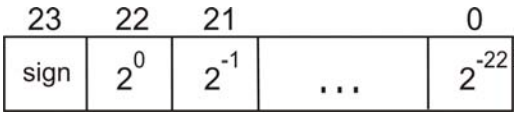

Figure 9. *Data format 2*

Examples:

Ioff= $(1\text{-}2^{-23})$dec = (0111 1111 1111 1111 1111 1111)bin=(8FFFFF)hex

Igain= $(2\text{-}2^{-22})$dec = (0111 1111 1111 1111 1111 1111)bin=(8FFFFF)hex

2.3.3 Communication Serial Port

The realized communication controller has to provide tuning, remote control and monitoring. It is designed as modification of standard I^2C interface. Basically, I^2C was primarily intended for master–slave communication, where master communicates to a number of slaves by addressing them individually. CSP test concept considers one master reading from and writing to internal memory words of one slave device – the PMIC prototype. Thus, master is not addressing the slave units, but individual words within the PMIC. Actually, only the DSP part of LEDA08 (IMPEG01)is developed with 64 internal 24-bit words and one 24-bit command/status register. Thereby, 7-bit address format was adequate to address all the words in the chip.

Features of the realized CSP controller are:

- Performance in slave mode;
- Data transfer of 400 kbit/s (f_{SCL} = 400 kHz);
- 7-bit addressing;
- Filtering of incoming data from SDA and SCL lines;
- Detection of START, STOP and REPEATED START conditions;
- Latching of serial data bits from the SDA line with every falling edge of the SCL clock;
- 4-byte communication protocol;
- Synchronization with DSP part of the chip;
- Synchronization with master (inserting Wait-states).

In CSP-bus communication master initiates data transfer and generates serial clock signal

on the SCL line]. Since there is no need for the PMIC to initiate the transfer, only the slave mode is supported. We decided to use 400 kHz SCL frequency, because it gives us the ability to read all sampled data from the measurement part of the chip every second.

2.3.4 Registry Bank

The registry bank is based on 64 x 64 bit RAM. Table 3 presents the list of 55 registers accessible to user together with associated addresses.

Table 3 ***Table of registers***

	Name	Hex. Addr	Abbreviation
1	Instantaneous value of current, *i(t)*	(01)h	I
2	Instantaneous value of voltage, *v(t)*	(02)h	V
3	Instantaneous voltage value phase shifted for 90 deg, *v'(t)*	(03)h	Vpom
4	MSB part of accumulator for Active Energy, E_{Aacc}	(04)h	AccEamsb
5	LSB part of accumulator for Active Energy, E_{Aacc}	(05)h	AccEalsb
6	MSB part of accumulator for Reactive Energy, E_{Qacc}	(06)h	AccEqmsb
7	LSB part of accumulator for Reactive Energy, E_{Qacc}	(07)h	AccEqlsb
8	MSB part of accumulator for inst. current square, $i_{acc}^2(t)$	(08)h	AccIImsb
9	LSB part of accumulator for inst. current square, $i_{acc}^2(t)$	(09)h	AccIIlsb
10	MSB part of accumulator for inst. active power, $p_{acc}(t)$	(0A)h	AccPmsb
11	LSB part of accumulator for inst. active power, $p_{acc}(t)$	(0B)h	AccPlsb
12	MSB part of accumulator for inst. reactive power, $q_{acc}(t)$	(0C)h	AccQmsb
13	LSB part of accumulator for inst. reactive power, $q_{acc}(t)$	(0D)h	AccQlsb
14	MSB part of accumulator for inst voltage square, $v_{acc}^2(t)$	(0E)h	AccUUmsb
15	LSB part of accumulator for inst. voltage square, $v_{acc}^2(t)$	(0F)h	AccUUlsb
16	MSB part of filter reg. for inst. current square, $i_{NF}^2(t)$	(10)h	YzIImsb
17	LSB part of filter reg. for inst. current square, $i_{NF}^2(t)$	(11)h	YzIIlsb
18	MSB part of filter reg. for inst. active power, $p_{NF}(t)$	(12)h	YzPmsb
19	LSB part of filter reg. for inst. active power, $p_{NF}(t)$	(13)h	YzPlsb
20	MSB part of filter reg. for inst. reactive power, $q_{NF}(t)$	(14)h	YzQmsb
21	LSB part of filter reg. for inst. reactive power, $q_{NF}(t)$	(15)h	YzQlsb
22	MSB part of filter reg. for inst voltage square, $v_{NF}^2(t)$	(16)h	YzUUmsb
23	LSB part of filter reg. for inst. voltage square, $v_{NF}^2(t)$	(17)h	YzUUlsb
24	Gain correction for RMS current, I_{gain}	(18)h	Igain

25	Gain correction for RMS voltage, V_{gain}	(19)h	Vgain
26	Gain correction for average active power, P_{gain}	(1A)h	Pgain
27	Offset correction for RMS current, I_{off}	(1B)h	Ioffset
28	Offset correction for RMS voltage, V_{off}	(1C)h	Voffset
29	Offset correction for average active power, P_{off}	(1D)h	Poffset
30	Offset correction for average reactive power, Q_{off}	(1E)h	Qoffset
31	RMS current, *I*	(1F)h	Irms
32	RMS voltage, *V*	(20)h	Vrms
33	Average active power, *P*	(21)h	P
34	Average reactive power, *Q*	(22)h	Q
35	Apparent power, *S*	(23)h	S
36	Power factor, *cos(φ)*	(24)h	Cos(φ)
37	MSB part of reg. for generated impulses for negative Active energy, $-E_A$	(25)h	WhrNegEamsb
38	LSB part of reg. for generated impulses for negative Active energy, $-E_A$	(26)h	WhrNegEalsb
39	MSB part of reg. for generated impulses for negative Reactive energy, $-E_Q$	(27)h	WhrNegEqmsb
40	LSB part of reg. for generated impulses for negative Reactive energy, $-E_Q$	(28)h	WhrNegEqlsb
41	MSB part of reg. for generated impulses for positive Active energy, $+E_A$	(29)h	WhrPosEamsb
42	LSB part of reg. for generated impulses for positive Active energy, $+E_A$	(2A)h	WhrPosEalsb
43	MSB part of reg. for generated impulses for positive Reactive energy, $+E_Q$	(2B)h	WhrPosEqmsb
44	LSB part of reg. for generated impulses for positive Reactive energy, $+E_Q$	(2C)h	WhrPosEqlsb
45	Correction reg. for pulse generation on EOUT pin, *WhrReg*	(2D)h	Whr_corr
46	Correction reg. for frequency calculation,	(2E)h	Freq_imp
47	Frequency, *f*	(2F)h	Freq
48	Gain correction for average reactive power, *Qgain*	(30)h	Qgain
49	First operand for testing purpose	(31)h	POD1
50	Second operand for testing purpose	(32)h	POD2
51	Third operand for testing purpose	(33)h	POD3
5	First result for testing purpose	(34)h	REZ1

2			
53	Second result for testing purpose	(35)h	REZ2
54	Register for phase offset calibrating between instantaneous current and voltage samples	(FF)h	ConfR
55	Status register	(FE)h	Status

3. BIAS CONDITIONS

LEDA08 (IMPEG01) is a prototyped in AMI Semiconductor CMOS 0.35um technology. C035M technology family is designed for 3.3 volt (+0.3/-0.6 volt) power supply operation and consequently, VDD-VSS biasing have to fulfill the specified condition.

4. PINOUT

As LEDA08 (IMPEG01) is a prototype and a test chip, it has numerous test pins. In order to distinct them from other pins they are denoted in italic letters in the pin list given in Table 4. The chip is assembled in DIL 40 case shown in Figure 10.

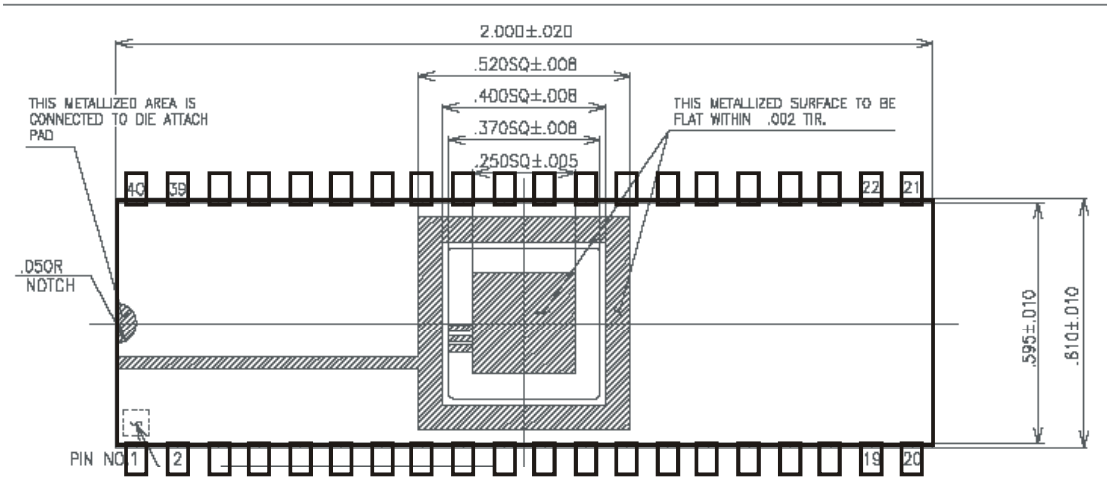

Figure 10. Package DIL 40

Table 4 ***Pin list***

Pin #	Symbol	Description	Note
1	XOUT	Quartz output	
2	*CLK/8*	Output, with a clock divided by 8	(for testing only, NC otherwise)
3	VDDI1(VD+1)	Digital VDD	
4	VSSI1(DGND)	Digital Ground	
5	SCLK	Clock for CSP	
6	SDA	Serial Data Access for CSP	

7	CS	Chip select for CSP	(Enabled with logic 0)
8	VDDE - Digital VDD		
9	VDDI2(VD+2)	Digital VDD	
10	VSSI2(DGND2)	Digital GND	
11	*VINT*	inout, alternative input or output for the voltage samples from ADC	(for testing only, NC otherwise)
12	NC		
13	GNDRING	Ground for Guard Ring	
14	VDDCO2(VA+2)	Analog VDD for bandgap reference	
15	VSSCO2(VA-2)	Analog VSS for bandgap reference	
16	VIN+	+ input for Voltage channal	
17	VIN-	- input for Voltage channal	
18	*VREFIN1*	Buffered reference voltage input	(for testing only, NC otherwise)
19	VREFOUT	Bandgap output	(in normal operation shorted with VREFIN)
20	VREFIN	Reference voltage input	(for external voltage reference)
21	*VCMI*	Common mode input for ADC	(for testing only, NC otherwise)
22	VSSCO1(VA-1)	Analog GND	
23	VDDCO1(VA+1)	Analog VDD	
24	IIN-	- input for Current channel	
25	IIN+ Analog	+ input for Current channel	
26	*AN0*	Analog + output of integrators	(for testing only, NC otherwise)
27	*AN1*	Analog output of integrators	(for testing only, NC otherwise)
28	*CTRL0*	Control signal for AMUX	(for testing only, 0 otherwise)
29	*CTRL1*	Control signal for AMUX	(for testing only, 0 otherwise)
30	*IINT2*	Inout, alternative input or output for the current samples from ADC	(for testing only, NC otherwise)
31	*IINT1*	Inout, alternative input or output for the current samples from ADC	(for testing only, NC otherwise)
32	*ADEN*	Control signal for orientation of VINT, IINT1 and IINT2	(for testing only, 1 otherwise)
33	VSSE	Digital GND	
34	MODE0	Mode selection	See Table 1
35	MODE1	Mode selection	See Table 1
36	*RUN/STOP*	Controlling pin during the test mode	(for testing only, 0 otherwise)
37	EOUT	Output pin that generates a pulse on every Wh	
38	ERROR	Output pin that generates a pulse on every error	
39	*1SEC*	Output pin that generates a pulse on every second	(for testing only, NC otherwise)
40	XIN	Quartz input	