

TESTING SET-UP FOR ANALOG PART OF THE POWER-METER IC

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The set-up and testing procedure for the analog part of the mixed signal ASIC dedicated for power-metering together with the obtained test results are presented in this paper. Apart from DFT techniques implemented in the IC, testing set-up was required. It was essential to provide an efficient and inexpensive test set-up which does not require large industry testing equipment.

1. INTRODUCTION

In order to successfully develop one integrated system on chip, invention and implementation of new circuits is as important as the testability of the prototype chips. Every fabricated integrated circuit requires a separate test set-up for supplying it with the power, clock and input signals, testing chips' contacts and, finally, verification of the entire functionality. Checking the accomplishment of all specifications requires complex and noiseless analog test signals as well as the monitoring of the chip real-time response. It is very desirable for the test execution to be PC controlled, and to have a capability to easily adjust the software and hardware. For confirming the correct functioning of the device and for enabling the device characterization, testing approach has to be developed in order to interface the device to be tested and the testing and measuring equipment. This protocol must ensure transferring the large number of different signals. The test set-up itself should have the capability of manual as well as PC control and should also be attainable for other similar purposes [1].

Beside this, one very important issue considering prototype testing is its cost. Industry testers are very expensive and require special conditions and a lot of space. Laboratory measurements and prototype testing should not be that costly, since the chip prototyping is already very expensive.

One test set-up solution dedicated to the analog part of the power-meter IC testing is presented in this paper. The test set-up was developed agreeably to DFT (Design For Testability) solutions integrated into the analog part of the chip.

The paper will be organized as follows. In the second chapter a short description of the analog part of the chip, building blocks and functionality will be given. A special attention to the specific DFT techniques that enable test set-up developing, as well as testing itself will be described. Third chapter deals with the test set-up. It was necessary to develop additional hardware, as well as data acquisition card control software. Testing procedures will be explained in the fourth chapter. In the last chapter some test results will be given.

2. EMBEDDED ANALOG DFT TECHNIQUES IN INTEGRATED POWER-METER

The power-meter IC consists of analog and digital part [2]. Architecture of the analog part of the chip is shown in Figure 1. The main objective of the analog part of the IC is to perform A to D conversion of voltage and current input signals. The requirements for ADCs are dynamic range of at least 80dB in the current channel and 60dB in the voltage channel. Preferred bandwidth is 2 kHz with input sampling rate of 524.288 kHz. The input sinusoidal signal range is 250 mVpp with line frequency of 50 Hz. The specified features can be met using second order modulator in the voltage channel and a third order modulator in the current channel with one-bit digital signal at voltage and 2-bit signal at current line and with oversampling ratio of 128 in both channels. Basically the analog part consists of a bandgap circuit which is used as a voltage reference generator and two $\Sigma\Delta$ modulators built of SC integrator sections.

In order to enable testing and measurement of this part of the chip, digital signals have to be accessible together with some important analog signals. The proper choice of analog signals is of essential importance for good observability, especially for the chip prototype. The bandgap circuit provides necessary reference voltage levels for other blocks of analog part of the chip [3]. Its voltages are also available at the external pin of the chip ($V_{ref out}$) as shown in Figure 1. To insure the reference voltage level for modulators, an additional external pin ($V_{ref in}$) was added to be used in the case that internal bandgap does not function in a proper way, by inducing it from the external source.

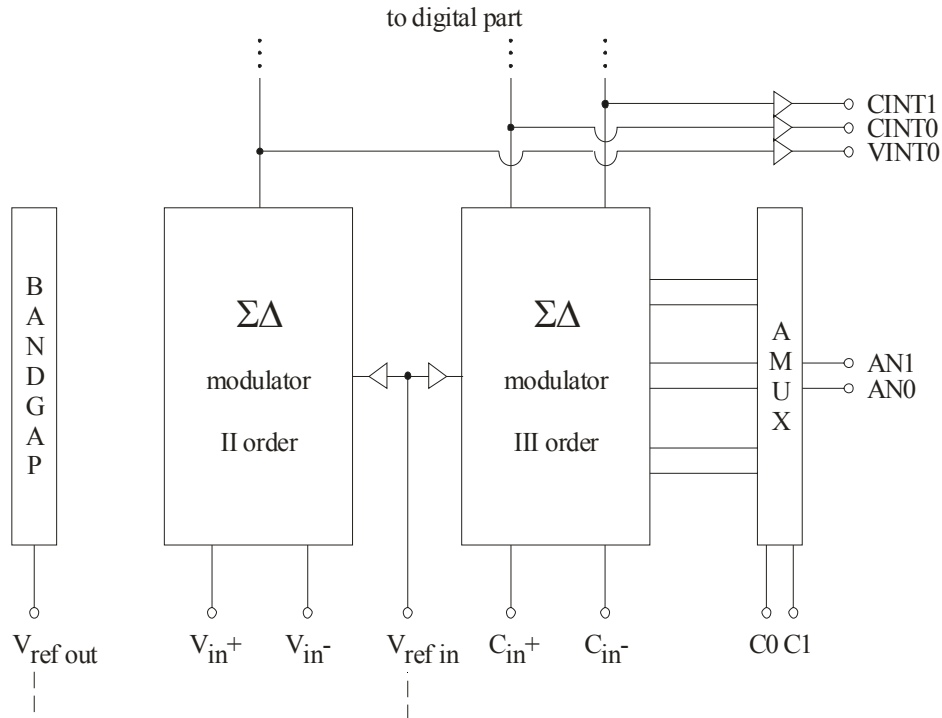


Fig. 1. Architecture of the analog part of the power-meter IC

Embedded DFT techniques improve testing capabilities of the analog part of the chip. The realization of this concept requires relatively simple hardware that consists

of: analog multiplexers, buffers and additional pins dedicated for testing. Output digital signals for both $\Sigma\Delta$ modulators can be viewed and collected at the digital bidirectional pins CINT0 and CINT1 for the current line, and VINT for the voltage line. These pins can also be used as input pins for signals brought from the external analog circuits in case that the analog part of the chip shows imperfections.

Since $\Sigma\Delta$ modulators are built of integrator stages, it is necessary to observe output signals of each integrator stage [4]. The third order $\Sigma\Delta$ modulator is designed as 2-1 MASH structure [5] that already contains the same second order $\Sigma\Delta$ modulator as used for the voltage channel. Therefore, monitoring internal signals in the third order $\Sigma\Delta$ modulator is sufficient for getting insight into behavior of every integrator stage. Analog multiplexer (AMUX in Figure 1) reduces number of added external pins. This multiplexer has 6 analog inputs collecting 3 differential signals from output of each integrator, 2 control input digital pins: C0 and C1, and 2 analog output pins: AN0 and AN1 where particular integrator differential output is observed.

3. TEST SET-UP FOR ANALOG PART OF THE POWER-METER IC

The test set-up for the analog part of the power meter IC is shown in Figure 2 [6]. This set-up enables testing of all analog blocks. It was developed using available hardware resources and contains: NI-DAQ PC-DIO-96 PnP acquisition card [7], SRAM cells, level shifters, signal conditioning circuit and control logic loaded into Xilinx FPGA chip XC4003E [8].

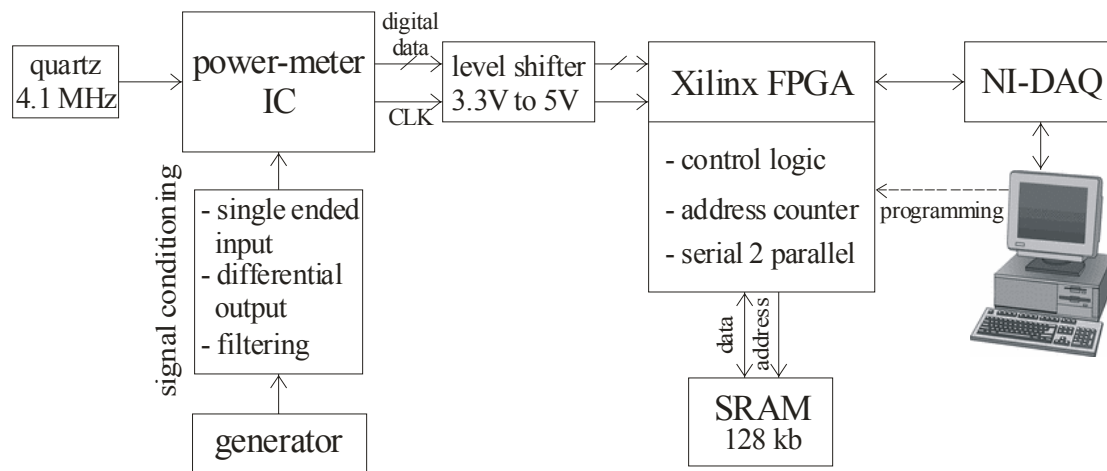


Fig. 2. Test set-up for analog part of the power-meter IC

There are several entities in the proposed test set-up. The first subunit is unit under test (the power-meter IC) with adjacent circuitry containing a quartz oscillator that provides clock frequency of 4.194MHz, small blocking capacitors connected to the pins for power supply, microswitches for setting operating mode of the chip, and buffers (unity gain operational amplifier) that interface observed pins with measuring equipment.

Second subunit provides signal conditioning. It converts a single ended analog input signal into differential signal required to drive analog input pins of the chip. Besides, it offers adjustable phase shift between voltage and current channels. In

order to reduce the noise and disturbances of the input signal, additional low-pass filter is also built in this circuit. The input signal is supplied by the low noise signal generator HP 3330B Automatic Synthesizer.

Xilinx XC4003E FPGA is programmed to control the data flow between unit under test, SRAM and NI-DAQ. There are four SRAM chips (UM61256-15) connected to provide total capacity of 4x32kx8 bits, which is enough for collecting digital data from the chip generated for 1 second during the normal operating mode. The FPGA converts serial to parallel data flow and generates appropriate address. It operates in two phases. During the first phase data flow from the power-meter IC through serial port to memory blocks. This action operates in real-time using the same clock as the IC. During the second phase the stored data move from SRAM through the NI-DAQ acquisition card into PC. This transfer occurs asynchronously by a specific hand-shake protocol. All necessary logic for this block was firstly described in VHDL, verified using the Active HDL simulator [9] and then programmed on Xilinx XC4300E FPGA device.

Since the power-meter provides logic levels of 3.3V and available Xilinx's FPGA and NI-DAQ acquisition card use 5V logic, it was necessary to insert level shifter circuits (74HC and 74HCT) between these two parts.

The subunit responsible for correct loading of collected data into the PC is NI-DAQ PC-DIO-96 acquisition card. The data transfer requires a specific hand-shake protocol, coded in C to program the acquisition card. The hand-shake occupies two lines for control signals IBUF (interrupt) and STB (acknowledge) while other 8 lines are used for parallel data transfer from the SRAM to the PC.

In addition to equipment already mentioned, it was very helpful having a reliable oscilloscope during the test setting up. Here, a Tektronix TDS 210 digital real-time oscilloscope was used.

All equipment used here is relatively cheap. One spectrum analyzer which deals with low frequency signals could also manage testing, but is far more expensive than the developed set-up.

4. TESTING PROCEDURES

Procedures used for testing the analog part can be divided into the following steps.

The most important is collecting the digital data from the output of the analog part of the chip. To do this a differential sinusoidal (50Hz) signal with the amplitude of at most 250 mVpp has to be brought into the signal conditioning circuit. The output signal of this circuit is fed into already powered and clocked power-meter IC. Microswitches are in position to enable normal operating mode of the IC. The ADC generates one-bit signal for the voltage channel and two-bits signal for the current channel that are observable through bidirectional ports VINT, CINT0 and CINT1.

Now, control logic from the FPGA switches SRAM blocks to real-time data storing mode. After one second, all data are collected. Then, the data can be transferred from to the PC, via the acquisition card. The control logic is now switched

to the asynchronous transferring mode and a hand-shake program from the PC can be executed. When done, digital samples are stored into a file on PC and can be further analyzed.

This set-up can deal with different clock frequencies (up to 50MHz) and different amplitudes, shapes and frequencies of the input analog signal. It just might need few more additional SRAM cells in order to increase the amount of collected digital data.

Testing procedure cannot be finished here. Conclusions cannot be made over arrays of digital zeros and ones. In order to get insight into the work of ADC the FFT analysis has to be performed over the digital data. We used Matlab program package [10] to obtain required signal spectra.

The same test set-up also offers $\Sigma\Delta$ modulators' linearity testing. Here the testing procedure and the testing analysis would be similar.

This set-up enables observing voltage levels at the output of each integrator stage as well as the voltage level generated by the bandgap circuit.

5. RESULTS

Figure 3 shows the output spectrum of the second order modulator, obtained from the FFT of the acquired output of the modulator in voltage channel. Figure 4 presents obtained noise shaping of the second and third order modulator. It can be noted that the third order modulator suppresses noise better than the second one.

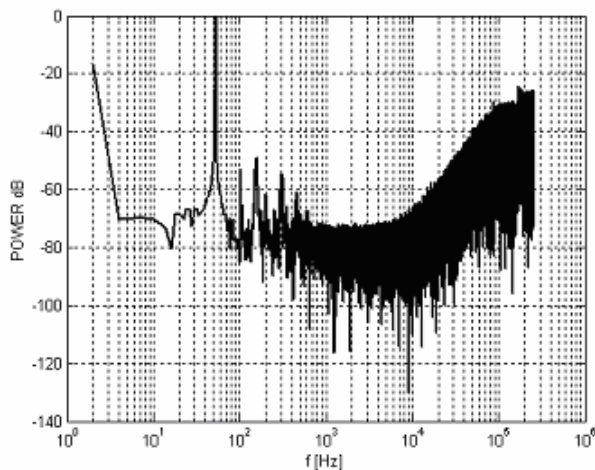


Fig. 3. Output spectrum of the second order modulator

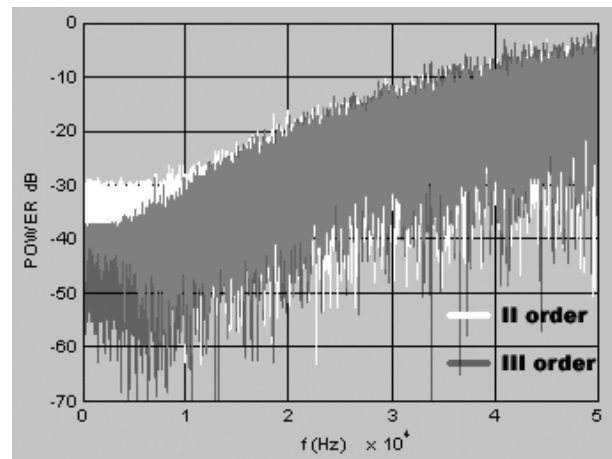


Fig. 4. Noise shaping

6. CONCLUSION

An application specific analog test set-up was presented in the paper. Test set-up developing involved both hardware and software solutions. This approach enables different levels of testing with variations of input signal: different amplitudes, phase shifts, frequencies, etc. The additional circuits implemented in the analog part of the chip improved the testability. This method offers functional oriented testing for a very low cost and a very simple manipulation. All fabricated power-meter IC samples are currently given for further industry testing.

7. REFERENCES

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