TESTING SET-UP FOR DIGITAL PART OF THE POWER-METER IC

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The testing problem in electronic circuit design does not include just DFT techniques on chip. In the laboratory environment it is also important to provide an efficient and inexpensive test set-up which does not require large industry testing equipment. This paper presents such a set-up and testing procedure for digital part of the mixed-signal ASIC dedicated for power-metering. The testing procedure consists of 2 levels: one during the normal operating mode and the second dedicated for particular testing of each arithmetic operator block. Control signals as well as the acquisition are performed through NI-DAQ PC-DIO-96 PnP card. All IC samples passed tests and are currently given for further industry implementation.

1. INTRODUCTION

The successful development of integrated systems on chip depends not only on inventing and implementing new circuits, but also on the testability of the prototypes. Every new chip needs a test set-up capable to provide safe power supply, to test its input and output interconnections, and to check the complete functionality. To fulfill all specified requirements the set-up needs particular hardware and software. Besides biasing, the hardware part has to provide stimulation of every input port and monitoring of the response in real time. Software part has to offer complex digital and analog patterns and appropriate testing algorithm that manages interface between the test equipment and the device under test. If one considers mixed signal chip he, obviously, must support a large number of signals. The signal flow is controlled by a certain protocol. Usually, the test facility has both manual and automated control and modularity for customizing the test set-up for a variety of applications [1].

On the other hand, it is also important that the prototype testing is not far costlier than the prototypes itself. This is particularly regarded to laboratory measurements and test set-ups. In this case avoiding the use of expensive and huge industry testers is very desirable or even obligatory.

This paper presents one application specific test set-up solution dedicated to the digital part of the power-meter IC [2]. It is developed according to corresponding *Design For Testability* (DFT) and *Design For Diagnostics* (DFD) techniques already incorporated into the digital part of the chip.

The paper is organized as follows. The second part gives a short description of functions and blocks built in the digital part of the chip. Specific DFT and DFD techniques that enable test set-up developing, as well as the testing itself will be

explained. The third section explains hardware of the test set-up while the fourth chapter describes testing procedures. A short overview of the protocol that enabled efficient data acquisition will also be given. In the last chapter some advantages of the used test set-up will be listed.

2. DFT AND DFD TECHNIQUES EMBEDDED IN DIGITAL PART OF THE POWER-METER IC

Architecture of the digital part of the chip is shown in Figure 1. It consists of two Decimation filters (for current and voltage channel), a Hilbert transformer, dedicated DSP part containing arithmetic blocks and a control unit, communication block, SRAM, and testing logic. It operates at f_c=4.194MHz. Decimation filters reduce sampling rate from $f_s=f_c/8$ to $f_s/1024$ and increase the data resolution from one bit up to 24 bits in the voltage and from two bits up to 24 bits in the current channel. The DSP calculates: current and voltage RMS values for the current and the voltage channel, power, energy and frequency of the input analog signal. The communication block manages I/O data exchange between ASIC and adjacent circuitry via two lines and in compliance to a special protocol.

According to the mixed-signal structure of the prototypes it was necessary to provide separate testing of analog and digital part. Moreover, that approach was mandatory due to the risk that analog part could not work. So, three bidirectional ports were left during design: one as digital I/O port for the voltage and two for the current channel.

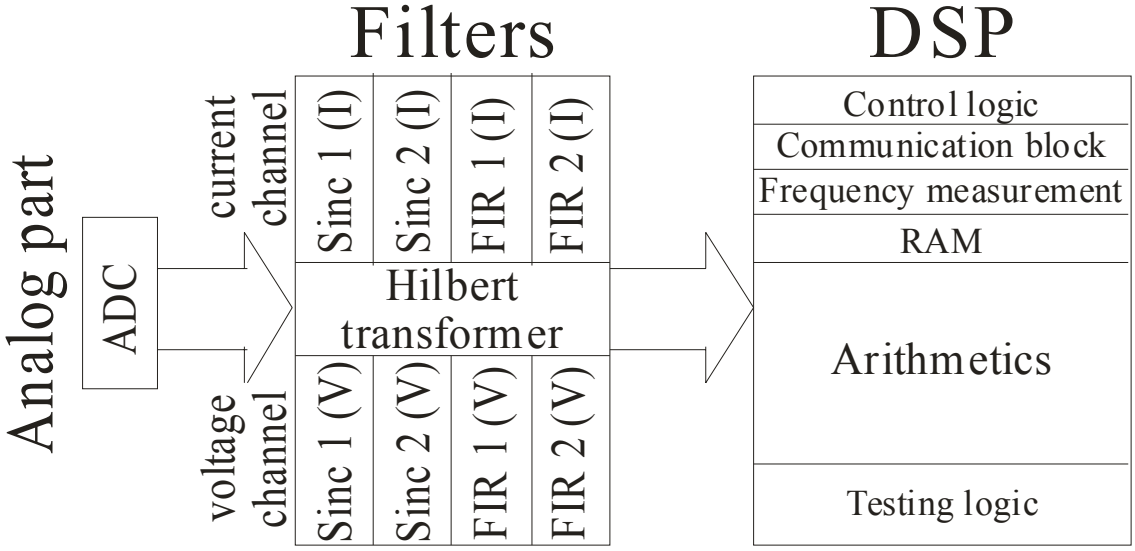

Fig. 1. Architecture of the digital part of the power-meter IC

Embedded DFT and DFD techniques improve testing and diagnostic capabilities of the chip. The realization of this concept requires relatively simple hardware that consists of: comparators, counters, data registers (which are also used in the system logic) and an additional status register which is a part of the register bank of the chip internal memory. This is shown in Figure 2 [3]. Generally, the aim of the test is to determine whether the operator under test functions properly.

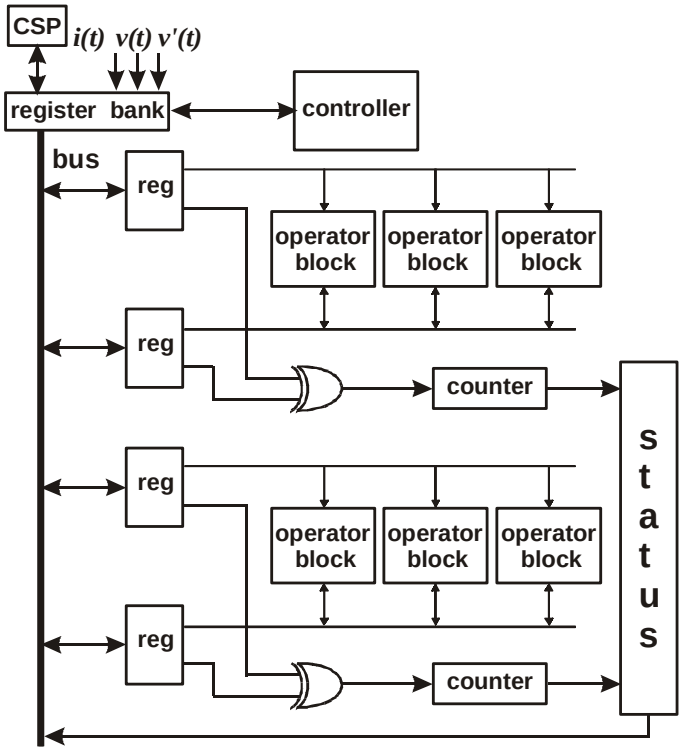

Fig. 2. Embedded DFT and DFD techniques of the digital part of the power-meter IC

The proposed testing approach assumes two main testing levels. One takes place during the normal operating mode, while the second one occurs throughout the special test mode. The chip switches to the test mode under special request of the user.

During testing in the normal operating mode, each operator keeps operands data in appropriate input registers. After processing, the obtained output, stored in the output register, is compared with the expected one. If the results match, the appropriate bit (corresponding to the operator under test) in status register keeps flag "0". However, two consecutively registered malfunctioning sets the bit to "1". Once written "1" in a certain bit position cannot be overwritten with another value until the *Status* register is read. This testing cycle repeats during normal operation mode in order to indicate the incorrect work of the DSP chain. Global testing cycle replicates the same procedure in order to enable access to each operation block, operands and result.

During the test mode detailed testing is enabled. All testing procedures will be explained in the forth section in detail.

3. TEST SET-UP FOR DIGITAL PART OF THE POWER-METER IC

The test set-up for the digital part of the power-meter IC is shown in Figure 3 [4]. Control signals are generated in PC and through NI-DAQ PC-DIO-96 PnP acquisition card loaded into chip [5]. This interface was also used for collecting results from IC stored within an internal RAM. During the normal operating mode DSP calculates all necessary power line signal parameters, once in 1s. Therefore, the minimal digital input test sequence needed to check DSP must contain data corresponding to 1s (50 periods of sinewave analog signals, presuming 50Hz power line).

ADC gives one-bit signal on the voltage channel and two-bit signal on the current channel after every rising edge of 512kHz clock. Consequently, one needs 3x512kb test vectors in order to provide required digital input signals.

During direct feeding the digital part with sequences generated by PC using the NI-DAQ card, a gap between the synchronous communication provided by the chip

and an asynchronous communication provided by the acquisition card, was observed. Thus, it was necessary to store the test pattern in the additional EPROM.

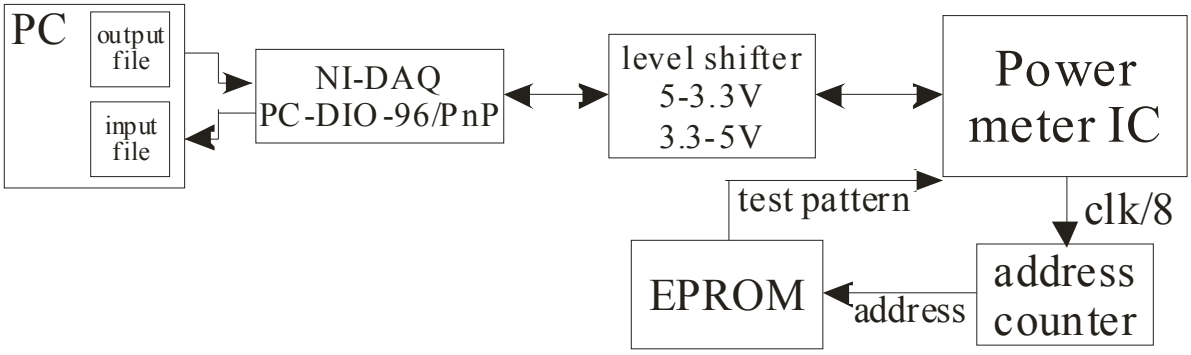

Fig. 3. Set-up for DSP testing

The additional EPROM has a capacity of 512k x 8 bits. This memory together with some logic blocks emulates the analog part of the chip. Test patterns for the current and the voltage signal occupy only 3 bits in each of 512k address locations available in the memory. So, the unoccupied memory space was used for storing the digital data of the phase shifted voltage signal. Available phase shifts are: 15^0, 30^0, 45^0, 60^0 and 90^0. The usage of the memory requires also the use of the additional counter and logic to generate appropriate memory addresses. The clock signal for this counter is generated in the IC.

The acquisition card and the power-meter IC have different operating logic levels. In order to adjust them it was essential to use some level shifter circuits that can convert levels in both directions. Here a standard 74HC and 74HCT chips were used.

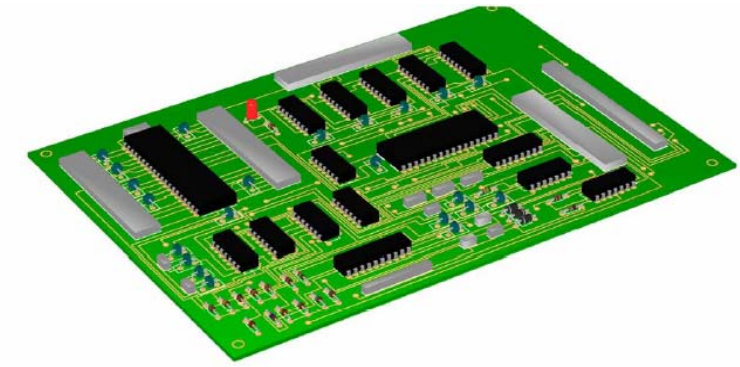

Fig. 4. The view of the testing board

Test patterns are obtained in the verification phase of the chip design. They are already used in simulations of the chip's digital part.

The circuitry described above was designed using program DXP-Protel and realized in a discrete manner on a separate printed circuit board. The view of the PCB is shown in Figure 4.

Considering the realized testing board, the desired communication protocol which was implemented in the chip and the available acquisition card, some special software solution had to be developed. These software solutions enable communication between the IC, that is, results written in the chip's internal memory locations, and a PC via the NI-DAQ acquisition card. All software solutions were written in C programming language.

4. TESTING PROCEDURES AND LEVELS OF TESTING

Testing procedure of the digital part consists of 2 levels. One is testing during the normal operating mode and the other is a detail testing of each operator block. This also corresponds to two operating modes of the chip: normal and test mode.

In the normal operating mode the testing of entire logic can be performed (correct functioning of the analog part of the chip is emulated using the external memory block), as well as the self-testing (checking if all arithmetic block calculate correctly).

The self testing procedure is the simplest one. It does not require test pattern loading into the chip. This procedure is performed every second during normal operation. The purpose of this procedure is to appoint if any of arithmetic operators in the chip works incorrectly. Operands and the correct results for this procedure are already stored in the ROM cell of the chip. The embedded logic within the chip compare expected results with the obtained one and marks a flag at the appropriate bit position of the Status register if a consecutive malfunctioning of an operator is detected. This Status register, as mentioned before, is a part of the internal memory register bank. If any of 9 arithmetic blocks does not function properly, it can be detected at the error pin of the chip, connected to an external led diode, in the case that the communication with a chip is not established, or, on the contrary, by reading the content of the status register over the developed interface. This is also regarded to as on-line testing since the testing sequences are incorporated in controller. In this case, no digital inputs are required. The testing at this level means observing the led diode connected to the error pin of the chip, or viewing the content of the status register after storing it in a PC. Software used for this purpose, controls different parameters of the DSP, such as gain correction, offsets, phase shifts and so on. Besides, it is feasible to drive digital inputs with signals corresponding to different shapes of analog signals. All these signals can be generated in PC, and then loaded into EPROM.

The next testing level stands for checking the entire DSP logic as well as the controller, especially if the previous test fails. Its purpose is to distinct if the defect occurs in the analog or the digital part. For this purpose the described testing board is inevitable. The EPROM keeps test patterns that emulate one second of correct functioning of the analog part. Therefore, input signals come from the memory instead from the analog part. Three additional pins intentionally left for testing allow this. The test pattern stored in the memory contains digital sequence input signal that corresponds to one second of regular operating. The testing implies the reading RAM contents through a serial port. Available data are: RMS values for current and voltage, power factor (cos φ), frequency, active, reactive and apparent power, energy, the status register and the state of the controller. Data collected from the developed testing board are memorized as a file into PC through the corresponding NI-DAQ interface (Figure 3). Finally, these results are compared with the expected, obtained by simulation.

The objective of the last testing level is to segregate particular arithmetic block responsible for incorrect DSP action. The chip has to operate in the test mode. Time

windows in the controller states are left and start/stop options are introduced to allow direct access to operand values for particular arithmetic blocks. Actually the user has permission to write desired values in the adequate memory locations, as well as to read results from the memory. Test patterns now may come directly from the PC, and through the acquisition card but not from the EPROM, because timing and synchronization problems do not exist. This testing level is capable not only to detect a failure but also to help in diagnosis using fault analysis techniques [6].

5. CONCLUSION

One specific application test set-up was presented in this paper. It implied both hardware and software development. This approach enables different levels of testing allowing variations of input signal: different amplitudes, phase shifts, frequencies, etc. The test logic implemented in the chip contains both DFT and DFD techniques and significantly simplifies the testing. It offers both functional and defect oriented testing. The advantage of this solution is very low cost and simple manipulation. All IC samples of the power-meter IC passed tests and are currently given for further industry implementation.

6. REFERENCES

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