TOP-LEVEL LAYOUT DESIGN OF SOLID-STATE ENERGY METER

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Abstract – *This paper presents top-level layout design of solid-state energy meter chip. The chip is mixed-signal, consisting of analog and digital part. The layout design flows for analog and digital blocks and top level are described. The solutions concerning blocks placement and routing, chip power planning and I/O ring construction are given.*

1. INTRODUCTION

Designers of complex integrated circuits and systems are unavoidably faced with many challenges. The complexity of problems rises if these systems are mixed-signal, containing both analog and digital part. This implies permanent cooperation among analog, digital, top-level layout, and test designers, in order to fulfill all the requirements needed.

In this paper layout design of solid-state energy meter is presented. It is a mixed-signal chip for active, reactive and apparent power measurement. Actually, the power is calculated as a product of measured voltage and current. Therefore the chip has two input channels, one corresponding to voltage, the other to current. The required dynamic range in current channel is greater than 80dB, while for voltage channel it is greater than 60dB. This implies that current channel is very noise sensitive. Therefore, it has to be separated from the voltage channel. The inputs to the system are two analog signals, later digitaly processed after A/D conversion, so the outputs are digital. This implies two main parts: analog and digital. The digital part consists of seven blocks operating at different clock frequencies. The highest clock frequency digital part is forced to be placed as far as possible from analog elements. Therefore, digital filters, operating at lower clock frequencies, are placed next to the analog part.

The next two sections consider problems and solutions related to layout design of analog and digital part, respectively. The fourth section discusses issues concerning the top-level design.

2. ANALOG PART OF THE CHIP

Analog part of the solid-state energy meter consists of following blocks: two sigma-delta modulators, bandgap voltage reference, two buffer circuits, and analog multiplexer. Modulator in current channel is implemented as a third-order (mash 2-1 structure) ΣΔ modulator, since dynamic of the input signal in the current channel is greater than in the voltage channel, where it is implemented as a second order modulator. Reference voltages are needed for the modulators to operate properly. These reference voltages are provided by the bandgap circuit. Its output is conditioned (buffered and level shifted) by the buffer blocks. Analog multiplexer enables output signals of modulator stages to be accessed outside the chip. It is implemented for testing purposes only.

Analog part of the circuit is very sensitive to noise. There are two ways in which digital noise can be transferred to analog part. One is through the substrate and the other is through the power supply lines. In order to minimize noise, analog part has separate power pads. Also, a ground ring, connected to separate pad is placed around analog part, in order to minimize substrate noise from the digital part.

Variations in bandgap reference voltage directly influence the errors in A/D conversion. In order to minimize noise in the bandgap circuitry, it is connected to separate supply pads.

Modulators, themselves, also include digital circuitry. Aiming to isolate other blocks from resulting noise, and also other analog noise, all analog blocks are surrounded with ground rings.

Digital noise occurs mostly on clock edges, as well as sampling in modulators. In order to provide steady signals on sampling instant, analog block is provided with clock which is shifted for T/4 in comparison to digital clock, where T is clock period.

Abstract layout of the analog blocks, containing necessary information for top-level placement and routing is generated from GDSII format in Cadence Abstract Generator program [1]. Table 1 presents dimensions for each analog block.

Table 1. *Analog Blocks Dimensions*

Block Name	*Dimensions*
Voltage A/D Converter	857.5um x 674.6um
Current A/D Converter	1024.3um x 652um
Analog multiplexer	153.6um x 103.5um
Bandgap voltage reference	177.9um x 173.9um
Analog Buffer	271.9um x 125um

3. DIGITAL PART OF THE CHIP

Seven blocks of digital part include:

1. DSP with control and communication logic
2. RAM macrocell provided by vendor
3. SINC filter in voltage channel
4. SINC filter in current channel
5. FIR filter in voltage channel

6. FIR filter in current channel

7. Hilbert transformer

Two first mentioned blocks operate at the highest clock rate defined by nominal frequency of an off-chip crystal oscilator, fo. The highest clock rate for each block is listed in Table 2.

Table 2. *Clock Frequency of Digital Blocks*

Block name	f_{clk}
DSP with control and communication logic	fo
RAM memory	fo
Current SINC filter	fo/8
Voltage SINC filter	fo/8
Voltage FIR filter	fo/256
Current FIR filter	fo/256
Hilbert transformer	fo/1024

Hilbert transformer is a FIR filter intended to introduce a constant phase shift of 90° in voltage signal in order to calculate reactive power. Voltage and current channel contain one decimation filter each, consisting of one SINC and one FIR filter. Low-pass SINC filters perform decimation in two stages with decimation factors 8 and 4, while two stages FIR filters are used for additional decimation with decimation factor 2 and additional correction of amplitude response. Output signals are then used to calculate rms values of voltage and current, active, reactive and apparent power, power factor and frequency. These values are stored in RAM memory.

Design flow of digital block layout generation in Cadence Silicon Ensemble is presented in Fig. 1, [2]. Before the process of physical layout generation can be started, an appropriate library database must be created. This library describes the target technology process for chip implementation. Importing several Library Exchange Format (LEF) files creates the library. These files are supplied by the silicon vendor and contain layer definitions, via definitions, via generation rules, appropriate design rules and information about cell shapes and connections. After the library database has been generated, importing synthesized Verilog netlists creates the design database.

The first step in place and route process is floorplanning. During this phase the parameters relating to the size and shape (square or rectangular) of the area where cells can be placed have to be specified. Before standard cells placement, the I/O pins are placed, in a way to make connections in top-level design as shorter as possible to avoid antenna violations [3]. After placing I/O pins, power rings should be constructed by specifying their distance from core, size and layer.

The next step is to place the standard cells in the rows. The clock tree is generated according to clock frequency time constraints, from the root pin to the clocked leaf pins. Filler cells are added to the design to fill the gaps in the peripheral rows. Filling the gaps, filler cells connect the power pins with their own internal layout. Filling the peripheral rows starts by inserting the widest filler cell and then reducing the width to the narrowest one, because this procedure minimizes the number of inserted cells.

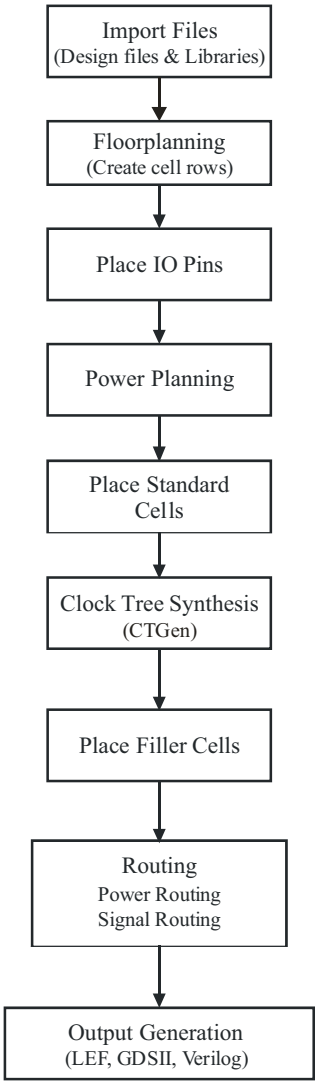

Fig. 1. Silicon Ensemble design flow for digital blocks

After the clock tree is built and filler cells are placed, the routing procedure may start. First, special routing is performed to connect block core to the power rings. Next step is to connect power pins of the standard cells within rows to the power rings.

Table 3. *Digital Blocks Dimensions*

Block Name	*Dimensions*
Hilbert transformer	865.5um x 967.5um
Voltage FIR filter	754.5um x 1084.5um
Current FIR filter	898.5um x 1048.5um
Voltage SINC filter	760.5um x 280.5um
Current SINC filter	901.5um x 322.5um

During the detailed routing the task of routing the signal nets in the block channel by channel is performed. During the several iterations the router optimizes the wire length and

number of vias. Thereafter, the design has to be checked for antenna violations, shorts and opens and design rules violations.

Finally, the design is exported to several different formats for further processing. The abstract layout of the block containing the layers and routing information that Silicon Ensemble needs to perform place and route, is saved in a LEF file. Besides, Verilog netlist is extracted in order to perform post-layout simulation.

Table 3 presents dimensions for each digital block.

4. TOP-LEVEL DESIGN

Top-level block placement is given in Fig. 2. First, analog and digital part are separated. The digital part operating at the highest clock frequency (DSP) is placed as far as possible from the analog part in order to minimize crosstalk. Blocks are grouped in voltage and current channel.

There are 39 I/O and power pads distributed evenly on four sides of the chip, as close as possible to corresponding pins. Obviously, the design is core limited. Different types of I/O pads are used: input, bidirectional and output for digital blocks and analog for analog blocks.

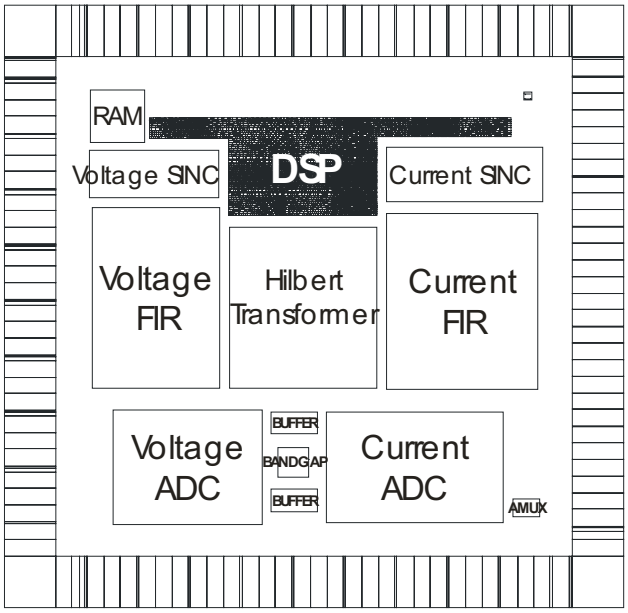

Fig.2. *Top-level placement*

Three types of power pads are used. VDDI and VSSI are internal supply and ground for core and I/O rings. The number of VDDI/VSSI pairs is a function of the core power consumption, frequency, peak currents, etc. VDDE and VSSE are external supply and ground for I/O rings only. The number of VDDE/VSSE pairs is a function of many parameters, such as package type, on-chip capacitance, I/O pad type, presence of analog blocks on chips, etc. VDDCO and VSSCO are internal supply and ground for analog core. The number of VDDCO/VSSCO pads is determined as for the VDDI/VSSI pads, depending on the current they are supposed to supply. Considering these remarks, there are two VDDI/VSSI pairs, one VDDE/VSSE pair and two VDDCO/VSSCO pairs. Since stability of bandgap voltage reference requires its own power supply, one VDDCO/VSSCO pair is used only for this purpose. Besides, a single VSSCO pad is connected to ground ring surrounding the analog part.

Power rings are constructed around each digital block. Moreover, the main power ring rounds the whole digital part and it is connected to power pads and all block rings. Power pads supplying analog blocks are interconnected directly to corresponding pins.

The algorithm for clock tree generation is based on user specified constraints, number of registers in the design and using a set of available buffers and inverters. The clock tree is constructed providing a number of clock signal clones. It is necessary to adjust minimum and maximum insertion delay and maximum clock skew in the constraints file according to the procedure described in [1]. Finally, it needs to be verified that there are no antenna or design rules violations.

Verified design is then exported to GDSII format used for further check and fabrication.

The area of the chip is 12.8mm^2, and the aspect ratio is adjusted according to block sizes. The target technology is AMI Semiconductor CMOS 0.35um [4].

Top-level layout is shown in Fig. 3.

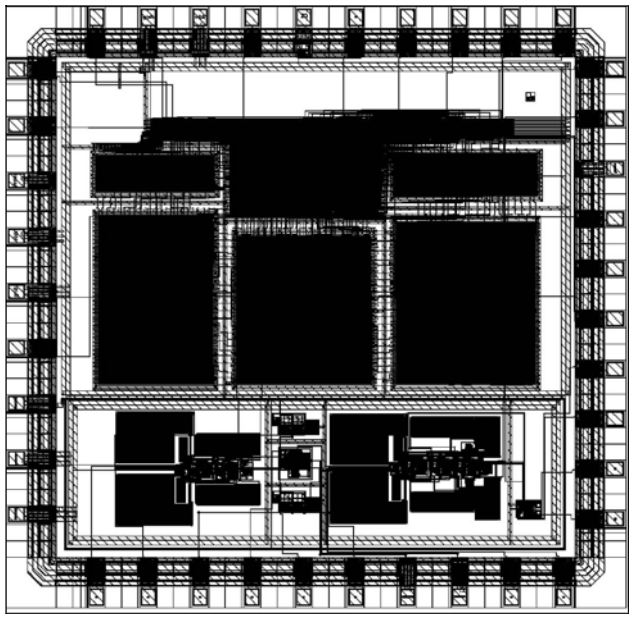

Fig.3. *Top-level layout*

5. CONCLUSION

Top-level layout design of solid-state energy meter is presented in this paper. Since the chip is mixed-signal, layout design process of both analog and digital part is described in more detail. The procedure of placing and interconnecting all blocks on the top-level, together with pads placing and power

rails construction is given. The prototype of the chip is delivered from manufacturing.

ACKNOWLEDGEMENT

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Sadržaj – U ovom radu predstavljen je postupak projektovanja lejauta integrisanog merača potrošnje električne energije. Kako se čip sastoji od analognog i digitalnog dela, opisan je proces projektovanja lejauta svakog od ovih delova. Data su rešenja koja se odnose na razmeštaj i povezivanje blokova, napajanje čipa i U/I prsten.

PROJEKTOVANJE LEJAUTA ZA INTEGRISANI MERAČ POTROŠNJE ELEKTRIČNE ENERGIJE

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