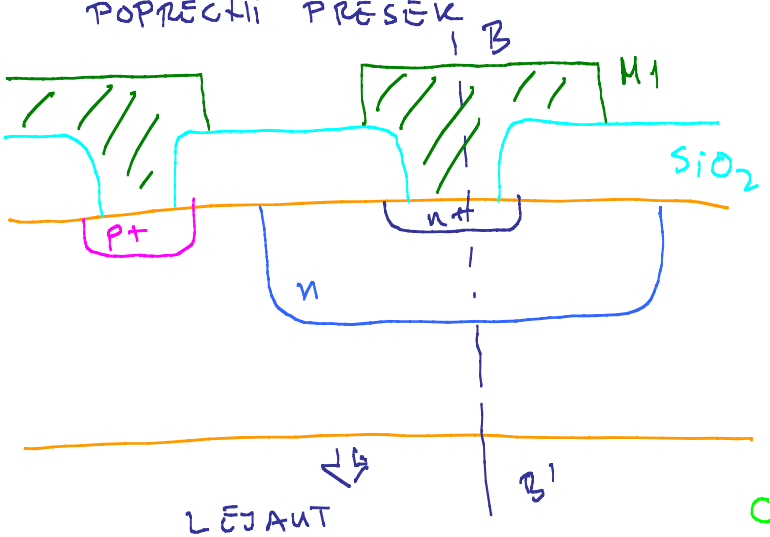
KOMPONENTE i MODELI

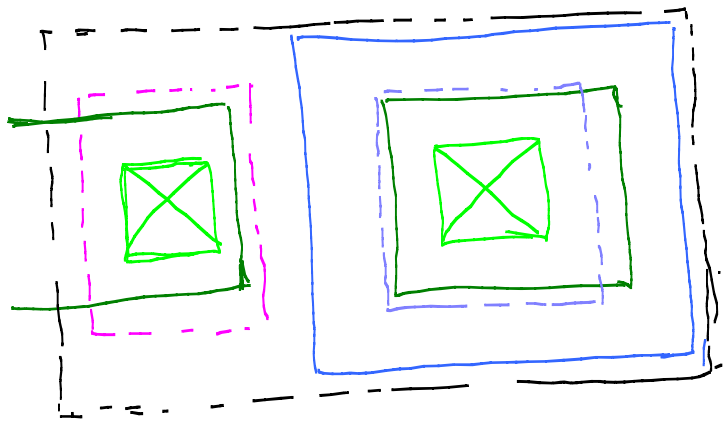
Note Title .8.5.2019

PN SPOJ (DIODA) U CMOS

POPREČNI PRESEK

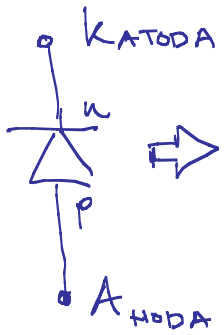


LEJAUT

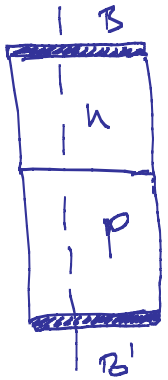


CONTACT
ACTIVE
N-WELL
N-PLUS – SELECT
P_PLUS-SELECT

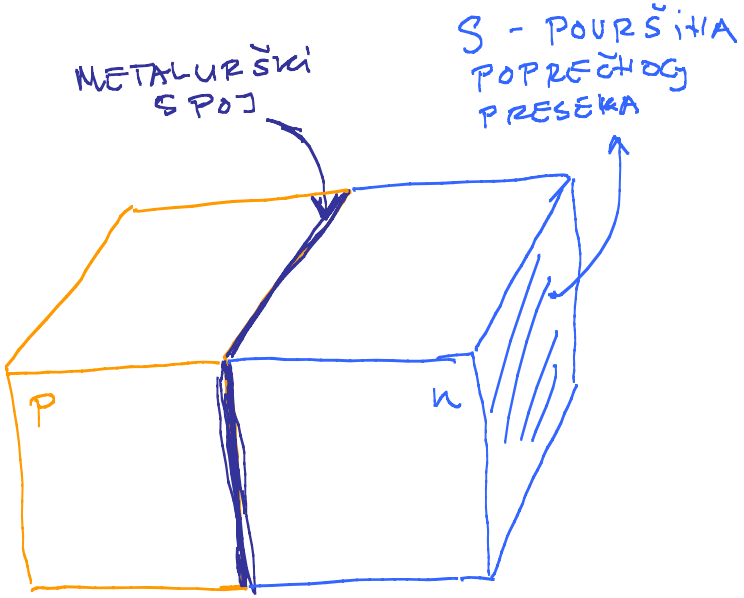
SIMBOL



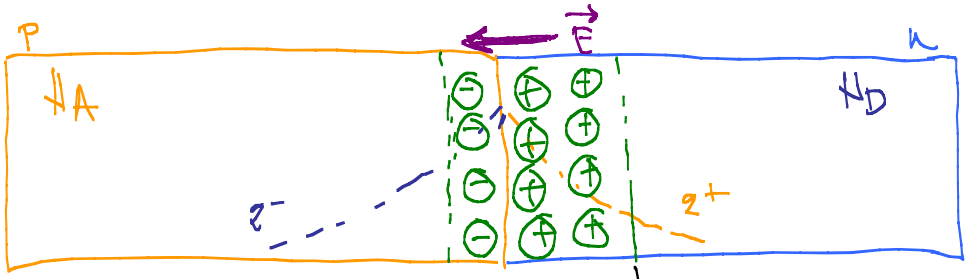
UPROŠĆEN 2D PRIKAZ



UPROŠĆEN 3D PRIKAZ



☐ NAELEKTRISANJE, POLJE, POTENCIJAL.



▷ PRETPOSTAVKE:

① „STRM" (ABRUPT) METALURŠKI SPOJ.

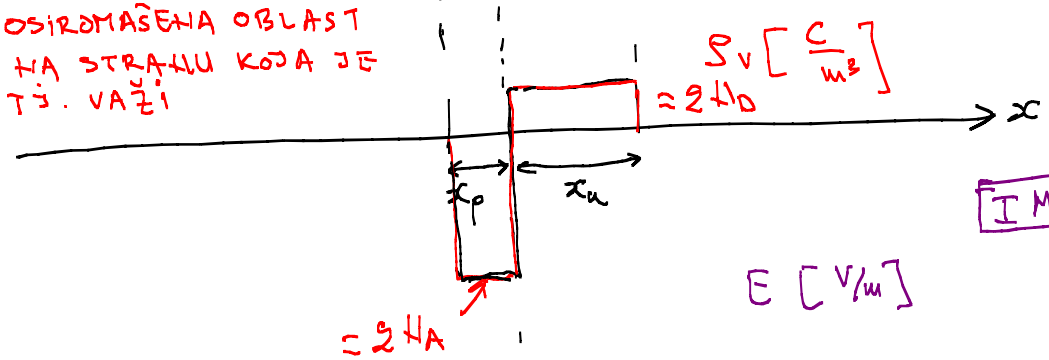
② $N_A > N_D$

③ KONSTANTAN POPREČNI PRESEK.

④ $E \neq f(S)$

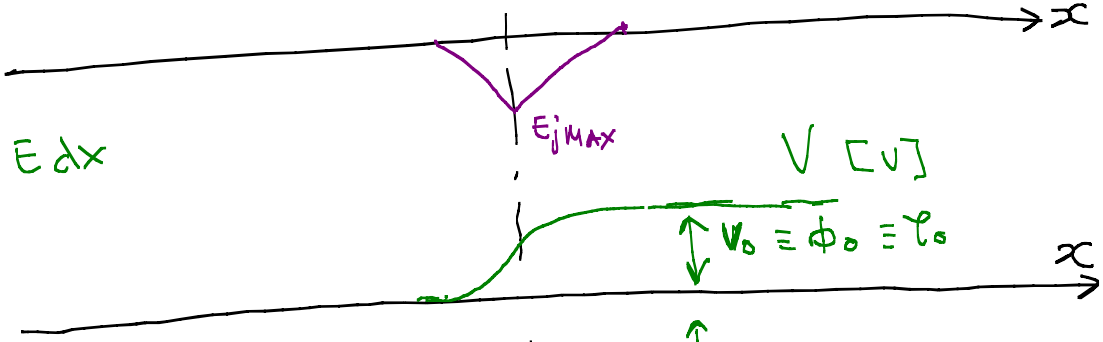
☐ ZAKON PN SPOJA: OSIROMAŠENA OBLAST SE VIŠE PROSTIRE NA STRANU KOJA JE MANJE DOPIRANA TJ. VAŽI

$$x_p N_A = x_n N_D$$

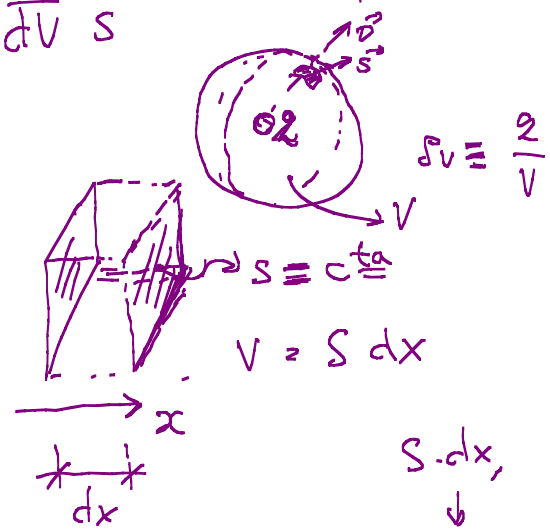


I MAX EQ. $\nabla D = \rho_v$, $D = \varepsilon E$, $\varepsilon \left[F/m\right]$

$E \left[V/m\right]$



$$\frac{d}{dV} \oint_S D\,ds = \rho_v$$



$$V = -\int E\,dx$$

$V \left[V\right]$

$$\varepsilon \oint_S E\,ds = \iiint_V \rho_v\,dV$$

$$V_T = \frac{kT}{q} \approx 26\,mV \;@\; T = 300\,K$$

V_0 – „UGRAĐENI" POTENCIJAL

$$V_0 = V_T \ln\left[\frac{N_A N_D}{n_i^2}\right] \quad (BUILT\text{-}IN)$$

n_i – „INTRINSIC" KONCENTRACIJA NOSILACA NAELEKTRISANJA U ČISTOM (NEDOPIRANOM) Si. $n_i \approx 10^{10} \frac{1}{cm^3}$ @ T=300K

$$\varepsilon E \cdot S = \rho \int \rho_v\,dx$$

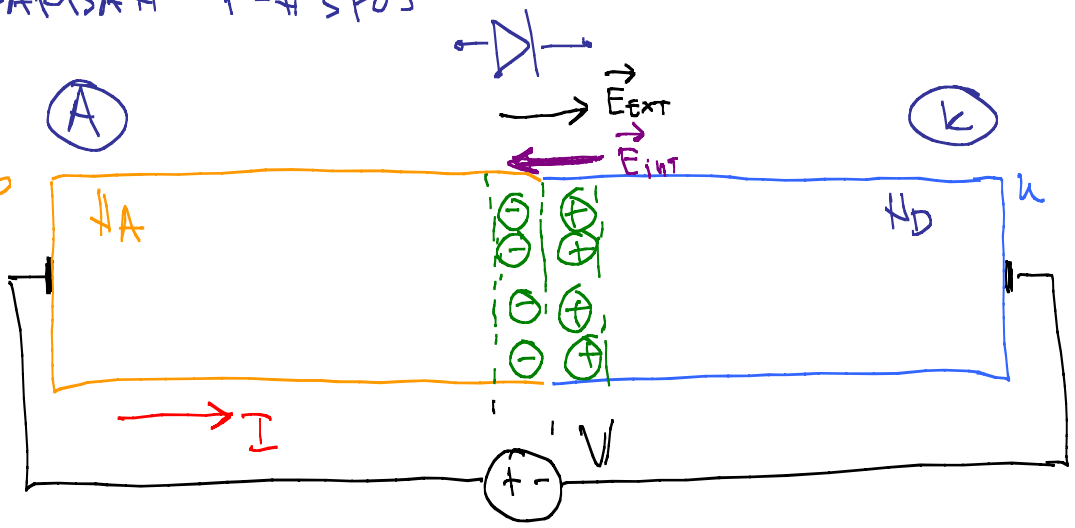
$$\boxed{E = \frac{1}{\varepsilon} \int \rho_v\,dx}$$

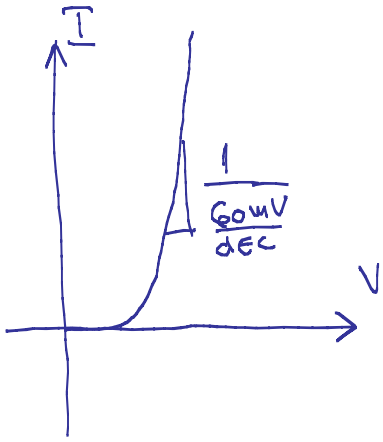
PRIMER 1: IZRAČUNATI V_0 AKO JE $N_A = 10^{15}/cm^3$, $N_D = 10^{14}/cm^3$ IN $T = 300\,K$

$$V_0 = 26\,mV \ln \frac{10^{15} \times 10^{14}}{10^{20}} = 26\,mV \times 9 \times \ln(10) = 538.8\,mV \blacksquare$$

$$V_0 \propto T$$

□ DIREKTNO POLARISAN P-N SPOJ





$$I = I_S \left(e^{V/V_T} - 1 \right)$$

I_S ↓ INVERZNA STRUJA ZASIĆENJA

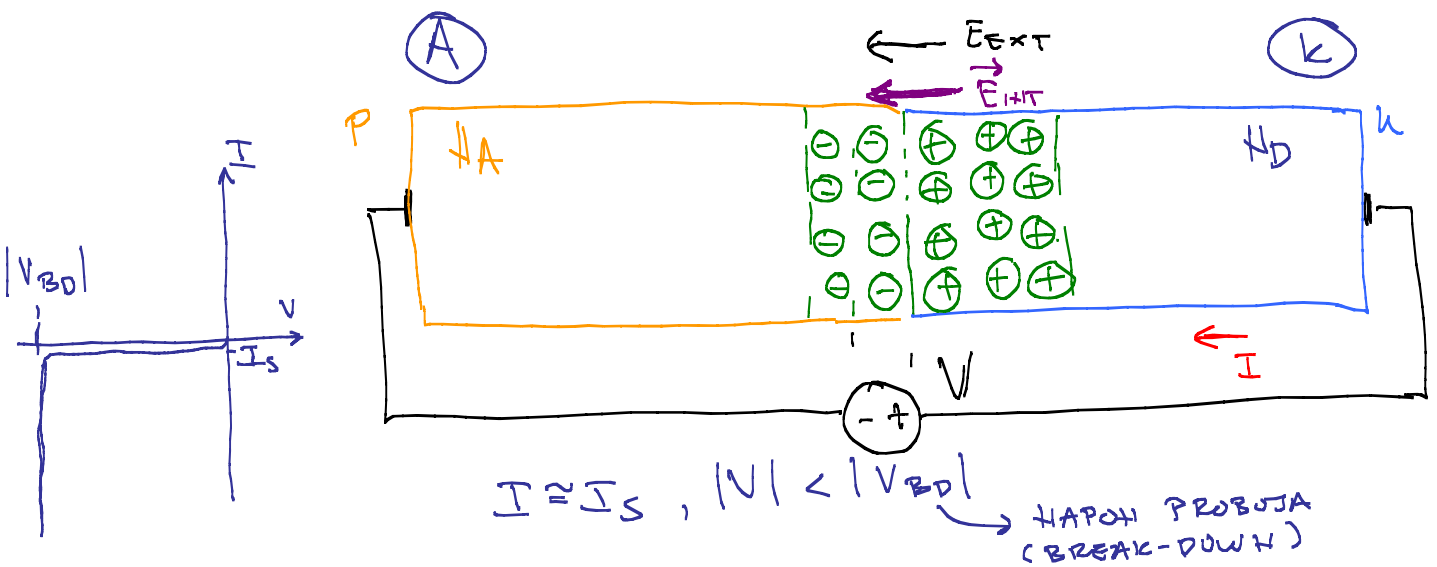
▷ $\text{sign}(\vec{E}_{EXT}) = -\text{sign}(\vec{E}_{INT})$

▷ OSIROMAŠENA OBLAST SE SMANJUJE

▷ SAVLADAVA SE POTENCIJALNA BARIJERA V_0 !

▷ PROTIČE ZNAČAJNA STRUJA I OD (A) KA (K).

□ INVERTNO POLARISAN PN SPOJ [U CMOS PN SPOJEVI UGLAVNOM INVERTNO POLARISANI !]



▷ $sign(\vec{E}_{EXT}) = sign(\vec{E}_{INT})$.

▷ OSIROMAŠENA OBLAST SE PROŠIRUJE.

▷ POVEĆAVA SE POTENCIJALNA BARIJERA.

▷ PROTIČE BEZNAČAJNO MALA STRUJA I OD (K) KA (A).

$I \simeq I_S$, $|V| < |V_{BD}|$ → NAPON PROBOJA (BREAK-DOWN)

□ NAELEKTRISANJE U OSIROMAŠENOJ OBLASTI:

$$Q_j = f(V_0 - V, N_A \| N_D, \varepsilon, 2, S) \; ; \quad N_A \| N_D = \frac{N_A N_D}{N_A + N_D}$$

S → POVRŠINA POPREČNOG PRESEKA PN SPOJA.

$$C \; [=] \; V, \; \frac{1}{m^3}, \; \frac{C}{V \cdot m}, \; C$$

$$Q_j = S\sqrt{2\varepsilon 2 (N_A \| N_D)(V_0 - V)}$$

□ MAKSIMALNO ELEKTRIČNO POLJE, E_{jmax}, NA SPOJU.

$$E_{jmax} = f(V_0 - V, N_A \| N_D, \varepsilon, 2)$$

$$\frac{V}{m} \; [=] \; V, \; \frac{1}{m^3}, \; \frac{C}{V \cdot m}, \; C$$

$$E_{|MAX} = \sqrt{2\frac{q}{\varepsilon}(N_A||N_D)(V_0 - V)}$$

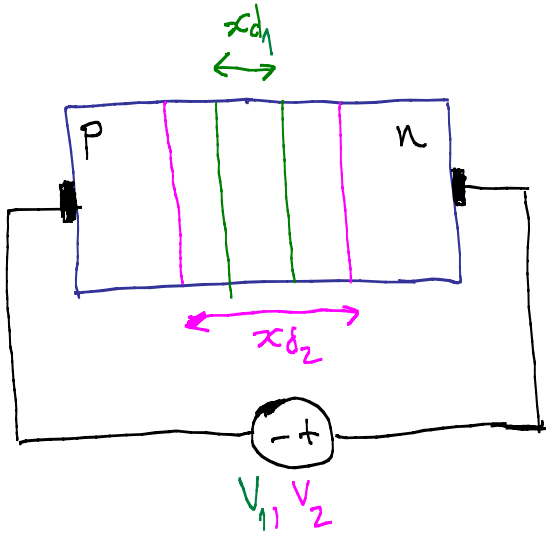
- Širina osiromašene oblasti

$$w\ [=]\ V,\ \frac{1}{m^3},\ \frac{C}{V\cdot m},\ C$$

$$x_d = x_p + x_n = \sqrt{2\frac{1}{(N_A||N_D)}\frac{\varepsilon}{2}(V_0 - V)}$$

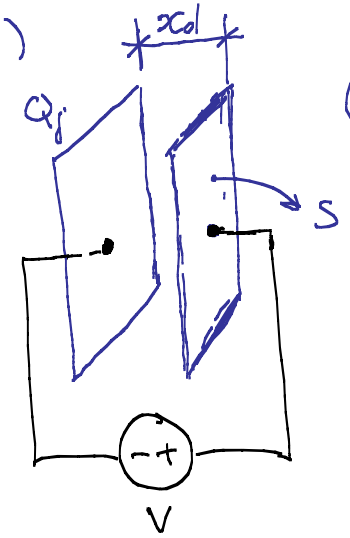
- VARIKAP DIODA (KAPACITIVNOST INVERZNO POLARISANOG PN SPOJA)

(KAPACITIVNOST "OSIROMAŠENE" OBLASTI - DEPLATION CAP)



$x_{d_2} > x_{d_1}$

$V_2 > V_1 \Rightarrow C_j \propto \frac{1}{V}$



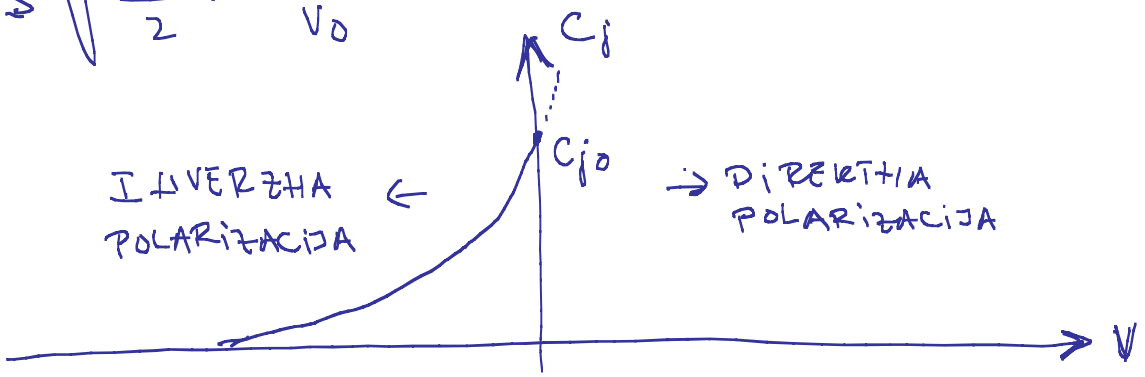
$$C = \varepsilon\frac{S}{x_d}$$

$$C_j = \frac{dQ_j}{dV} = \varepsilon \cdot \frac{S}{x_d} = \varepsilon S \sqrt{\frac{(N_A \| N_D)\, 2}{2\varepsilon} \frac{1}{(V_0 - V)}} = \frac{S}{\sqrt{1 - \frac{V}{V_0}}} \sqrt{\frac{\varepsilon 2}{2} \frac{(N_A \| N_D)}{V_0}}$$

$$C_j = \frac{C_{j0}}{\left(1 - \frac{V}{V_0}\right)^{m_j}} \quad ; \quad m_j = \begin{cases} 1/2 & \text{"STRM" PN SPOJ} \\ 1/3 & \text{"LINEAR" PN SPOJ} \end{cases}$$

$$C_{j0} = S \sqrt{\frac{\varepsilon 2}{2} \cdot \frac{(N_A \| N_D)}{V_0}}$$

C_{j0}



PRIMER 2: IZRAČUNATI KAPACITIVNOST INVERZNO POLARISANOG PN SPOJA POPREČNOG PRESEKA $S_j = 100\,\mu m^2$, KONCENTRACIJE AKCEPTORA $N_A = 10^{16}/cm^3$ I DONORA $N_D = 10^{17}/cm^3$ PRI NAPONU INVERZNE POLARIZACIJE $V = -1V$, NA SOBNOJ TEMPERATURI, $T = 300k$. PODRAZUMEVATI DA JE PN SPOJ LINEARAN I DA SE RADI O SILICIJUMU, $\varepsilon_{Si} = 11.68\,\varepsilon_0$.

$$V_0 = V_T \ln\left(\frac{N_A N_D}{n_i^2}\right) = 26mV \times \ln\frac{10^{16} \times 10^{17}}{10^{20}} = 26mV \times 13 \times \ln(10) \approx 26mV \times 13 \times 2.303$$

$V_0 = 778.27\,mV$; $N_A \| N_D \cong \frac{10^{33}}{11 \times 10^{16}} = \frac{10^{17}}{11} = 0.09 \times 10^{17} = 9 \times 10^{15}\ 1/cm^3 = 9 \times 10^{21}\ m^{-3}$

$$C_{j0} = S_{ij}\sqrt{\frac{2\varepsilon_{si}}{2V_0}(N_A \| N_D)} = 100 \times 10^{-12}\,m^2 \sqrt{\frac{1.609 \times 10^{-19}C \times 11.68 \times 8.85 \times 10^{-12}\,F/m}{2 \times 0.77827V} \times 9 \times 10^{21}\,m^{-3}}$$

$C_{j0} = 30.943\,fF$; LINEARAN SPOJ $\Rightarrow m_j = 1/3$

$$C_j = \frac{C_{j0}}{\left(1 - \frac{V}{V_0}\right)^{m_j}} = \frac{30.943\,fF}{\left(1 - \frac{(-1V)}{(0.77827V)}\right)^{1/3}} = 23.49\,fF$$

PRIMER 3 KOLIKA JE RELATIVNA RAZLIKA U KAPACITIVNOSTI IZ PRIMERA 2 AKO SE PREDPOSTAVI a) "STRM" PN SPOJ i b) $V = -2V$ i "LINEARAN" PN SPOJ [$C_{j\Sigma} = 23.49fF$]

a) "STRM" PN SPOJ $\Rightarrow m_j = 1/2$, $C_{j\Pi} = \frac{C_{j0}}{(1 - V/V_0)^{1/2}} = \frac{30.943fF}{\sqrt{1 + \frac{1}{0.77827}}} = 20.47\,fF$

$$\delta C_j = 100 \times \frac{|C_{j\Sigma} - C_{j\Pi}|}{C_{j\Sigma}} = 12.86\,\%$$

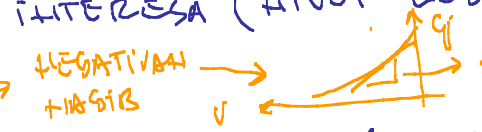
b) "LINEARAN" PN SPOJ $\Rightarrow m_j = \frac{1}{3}$, $C_{j\Pi} = \frac{C_{j0}}{(1 - V/V_0)^{m_j}} = \frac{30.943\,fF}{\left(1 - \frac{(-2)}{0.77827}\right)^{0.333}} = 20.25\,fF$

$$\delta C_j = 100 \times \frac{|C_{j\Sigma} - C_{j\Pi}|}{C_{j\Sigma}} = 13.82\,\%$$

KAPACITIVNOST INVERZNO POLARISANOG PN SPOJA ZA VELIKE SIGNALE

- C_j IZRAZITO NELINEARNA, POTREBAN JEDNOSTAVNIJI MODEL ZA ANALIZU I REDA.
- U DIGITALNIM KOLIMA UGL. JE DOVOLJNO PROCENITI SREDNJU VREDNOST KAPACITIVNOSTI, C_{jav}, ZA INTERVAL NAPONA OD INTERESA (NIVOI LOGIČKE NULE $|V_L|$ i JEDINICE $|V_H|$).

"STRMI" SPOJ ($m_j = 1/2$):



$$C_{jav} \equiv \frac{\Delta Q_j}{\Delta V} = -\frac{Q_j(V_H) - Q_j(V_L)}{V_H - V_L} = -\frac{Q_{jv}(V_0 - V_H)^{1/2} - Q_{jv}(V_0 - V_L)^{1/2}}{V_H - V_L}, \quad \{V_H, V_L\} < 0, \; |V_H| > |V_L|$$

$$Q_j = S\left[2\varepsilon q\,(N_A \| N_D)\,(V_0 - V)\right]^{1/2} = Q_{jv}(V_0 - V)^{1/2}; \quad Q_{jv} = S\sqrt{2\varepsilon q\,(N_A \| N_D)}\ \left[\frac{C}{\sqrt{V}}\right]$$

$$C_{j0} = S\left[\frac{\varepsilon q}{2V_0}(N_A \| N_D)\right]^{1/2} = \frac{1}{2} S\sqrt{2\varepsilon q\,(N_A \| N_D)}\,\frac{1}{\sqrt{V_0}} = \frac{1}{2} Q_{jv}\frac{1}{\sqrt{V_0}} \Rightarrow \boxed{Q_{jv} = 2\sqrt{V_0}\,C_{j0}}$$

$$C_{jav} = \underbrace{-2\sqrt{V_0}\,C_{j0}\,\frac{\sqrt{V_0 - V_H} - \sqrt{V_0 - V_L}}{V_H - V_L}}_{K_2} \Rightarrow \boxed{C_j = K_2\,C_{j0}}$$

$$K_2 = \frac{-V_0^{1/2}}{(V_H - V_L)^{1/2}}\left|(V_0 - V_H)^{1/2} - (V_0 - V_L)^{1/2}\right|$$

- U OPŠTEM SLUČAJU UMESTO $1/2 \to (1 - m_j)$ OSIM ZA $V_0^{1/2}$ GDE VAŽI $1/2 \to m_j$.

$$\boxed{K_2 = \frac{-V_0^{m_j}}{(V_H - V_L)(1 - m_j)}\left[(V_0 - V_H)^{(1-m_j)} - (V_0 - V_L)^{(1-m_j)}\right]}$$

$$m_j = \begin{cases} \frac{1}{2} & \text{ZA "STRMI" PN SPOJ} \\ \frac{1}{3} & \text{ZA "LINEARNI" PN SPOJ} \end{cases}$$

PRIMER 4 IZRAČUNATI SREDNJU VREDNOST KAPACITIVNOSTI INVERZNO POLARISANOG PN SPOJA AKO SE NAPON INVERZNE POLARIZACIJE MENJA U OPSEGU $[0.2\,V \div 0.9\,V]$. UZETI DA JE $V_0 = 0.65\,V$, $C_{j0} = 10\,fF$ I DA SE RADI O "LINEARNOM" PN SPOJU.

$V_L = -0.2\,V$,

$V_H = -0.9\,V$,

$m_y = 1/3$;

$$K_2 = -\frac{(0.65)^{1/3}}{(-0.9+0.2)\left(1-\frac{1}{3}\right)} \cdot \left[(0.65+0.9)^{(1-1/3)} - (0.65+0.2)^{(1-1/3)} \right] = 0.82$$

$$C_{jav} = K_2 \cdot C_{j0} = 8.2\,fF.$$

☐ IV KARAKTERISTIKA i MODELI.

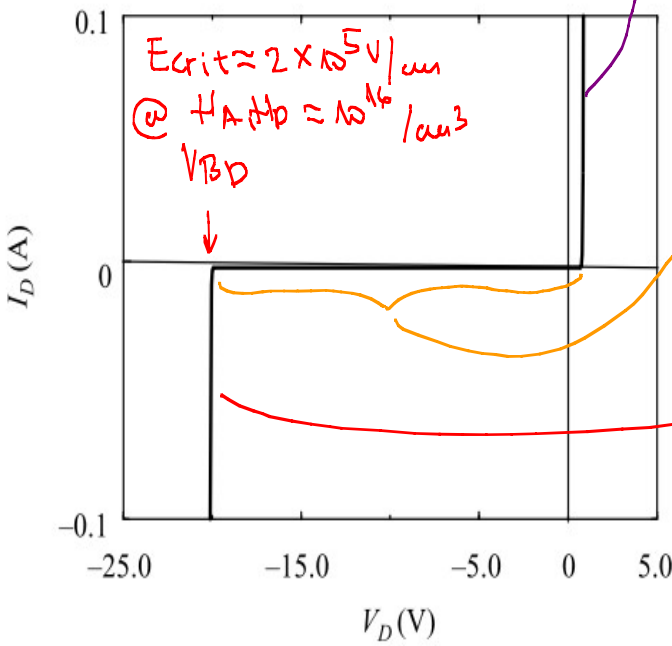
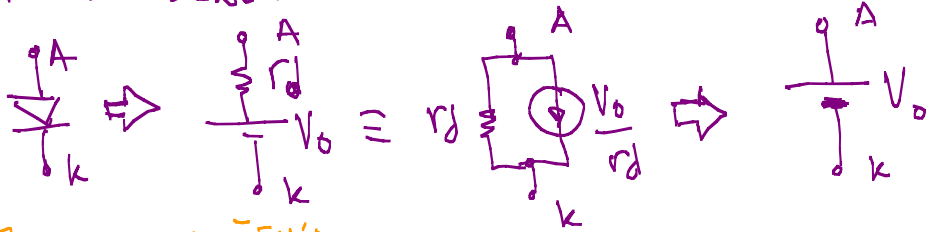
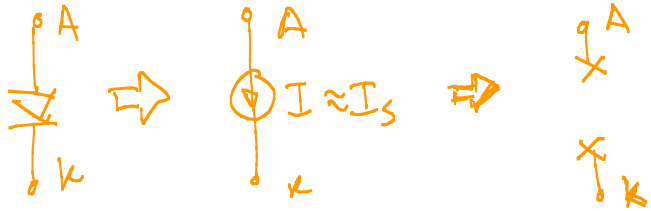


Figure 3.9 *I-V* characteristic of junction diode, showing breakdown under reverse-bias conditions (Breakdown voltage = 20 V).

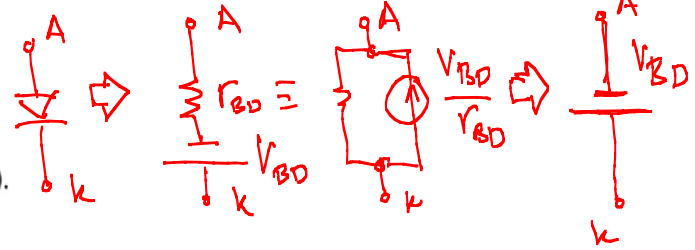
AKTIVNA OBLAST



OBLAST ZAKOČENJA



OBLAST PROBOJA (LAVINSKI ILI ZENEROV)

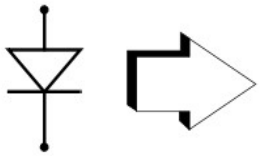


- IZRAZITA TEMPERATURNA ZAVISNOST: $V_T = \frac{kT}{q}$, $I_{S_1} \approx I_{S_0}\, 2^{\Delta T/10^\circ C}$ [$\Delta T = T_0 - T$, $I_{S_0} = I_S(T_0)$, $I_{S_1} = I_S(T_1)$]

PRIMER 5 KOLIKO PUTA SE UVEĆA INVERZNA STRUJA ZASIĆENJA AKO SE TEMPERATURA PROMENI ZA 20°C.

$\Delta T = 20^\circ C$, $I_{S_1} = I_{S_0}\, 2^{(20^\circ C/10^\circ C)} = 4 \times I_{S_0}$ ⇨ 4 PUTA.

- SPICE [SIMULATION PROGRAM WITH INTEGRATED CIRCUITS EMPHASIS] MODEL PN SPOJA [DIODA].



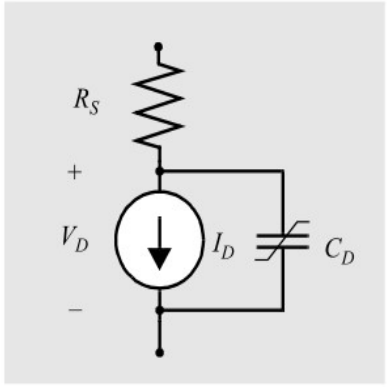


Figure 3.10 SPICE diode model.

$$I_D = I_S\left(e^{\frac{V_D}{nV_T}} - 1\right)$$

n - EMISIONI KOEFICIJENT

$$C_D = \frac{C_{j0}}{\left(1 - \frac{V_D}{V_0}\right)^{m_j}} + \frac{\tau_T I_S e^{V_D/nV_T}}{V_T}$$

- VIŠAK MANJINSKIH NOSILACA NAELEKTRISANJA. [EXCESS MINORITY CARRIERS CHARGE]. ISPOLJAVA SE PRILIKOM IZLASKA IZ AKTIVNE OBLASTI. POTREBNO JE KONAČNO VREME τ_T (TRANSIT TIME) DA SE NAGOMILANI MANJINSKI NOSIOCI UKLONE.

Table 3.1 First-order SPICE diode model parameters.

Parameter Name	Symbol	SPICE Name	Units	Default Value
Saturation current	I_S	IS	A	1.0 E−14
Emission coefficient	n	N	–	1
Series resistance	R_S	RS	Ω	0
Transit time	τ_T	TT	s	0
Zero-bias junction capacitance	C_{j0}	CJ0	F	0
Grading coefficient	m	M	–	0.5
Junction potential	ϕ_0	VJ	V	1

MOS-FET

METAL OXIDE SEMICONDUCTOR - FIELD EFFECT TRANSISTOR.

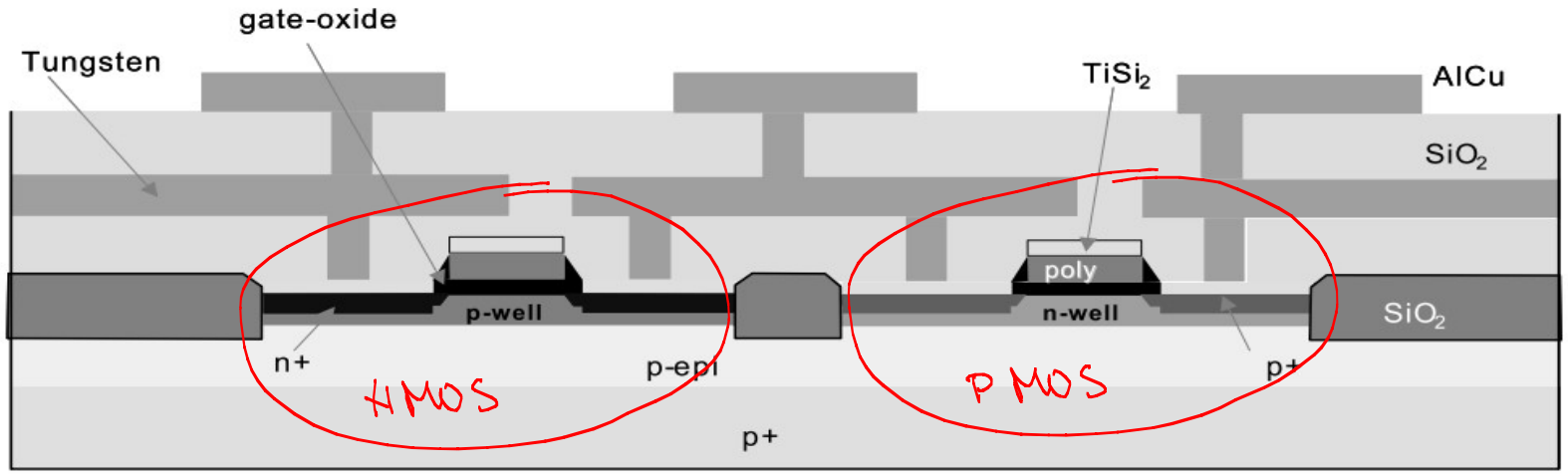
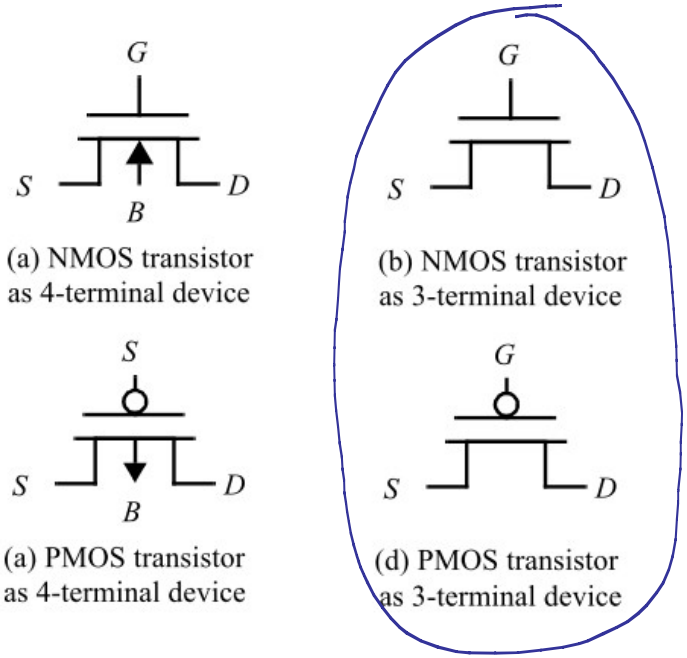


Figure 3.11 Cross-section of contemporary dual-well CMOS process.

☐ SIMBOL MOS-FETa U IC.



DU DIGITALNIM IC, AKO NIJE EKSPLICITNO OZNAČENO, PODRAZUMEVA SE DA JE OSNOVA (BALK) ZA:

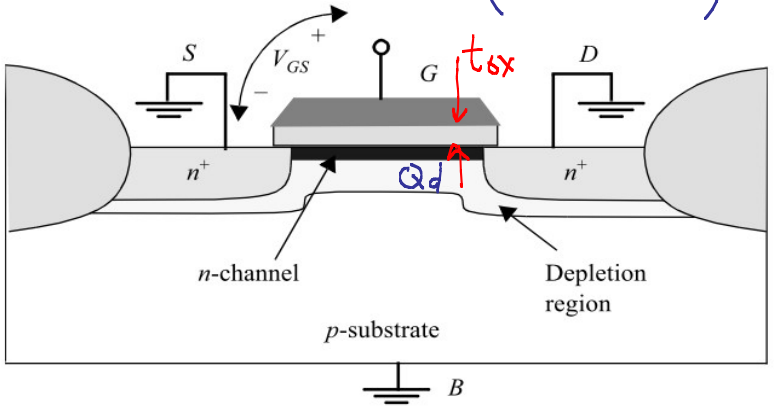
▷ NMOS POVEZANA ZA NAJNIŽI POTENCIJAL [OBIČNO MASA]. i

▷ PMOS POVEZANA ZA NAJVIŠI POTENCIJAL [OBIČNO NAPON NAPAJANJA].

☐ STATIČKA KARAKTERISTIKA MOS-FET-A.

▷ NAPON PRAGA (V_T)

NMOS (NACCNO)



- INVERZIJA PODRAZUMEVA KONTAKTNI POTENCIJAL $2\phi_F$ [ϕ_F – FERMIJEV POTENCIJAL].

$$Q_d = S\sqrt{2\varepsilon_{si}(N_A \| N_D)(2\phi_F)} = S\sqrt{2\varepsilon_{si} N_A (2\phi_F)}$$

$$\phi_F = V_T \ln\left(\frac{N_A}{n_i}\right) \approx 0.3\,V \text{ TIPIČNO}$$

$$x_d = \sqrt{2\frac{1}{(N_A \| N_D)}\frac{\varepsilon_{si}}{2}(2\phi_F)} = \sqrt{\frac{2\varepsilon_{si}}{2N_A}(2\phi_F)}$$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \left[F/\mu^2 \right], \quad \varepsilon_{ox} = \varepsilon_{r(SiO_2)} \varepsilon_0 \approx 4\varepsilon_0, \quad \varepsilon = \varepsilon_{r(Si)} \varepsilon_0 = 12\varepsilon_0, \quad \varepsilon_{r(Si)} = 11.68, \quad \varepsilon_{r(SiO_2)} = 3.9$$

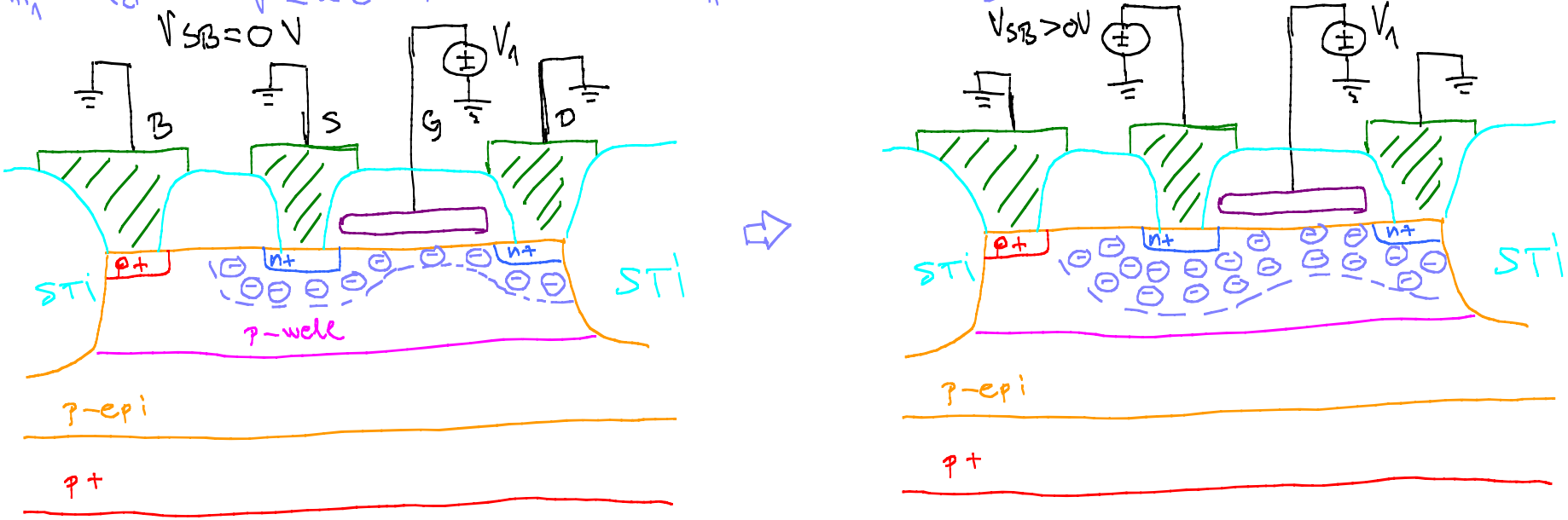
$$C \equiv \frac{dQ}{dV}, \quad V_T \propto \frac{Q_d/S}{C_{ox}} = \frac{\sqrt{2 q \varepsilon_{ox} N_A (2\phi_F)}}{C_{ox}} = \gamma \sqrt{2\phi_F}, \quad \gamma = \frac{\sqrt{2 q \varepsilon N_A}}{C_{ox}} \left[\sqrt{V} \right]$$

NAPON "RAVNIH TRAKA" (FLAT-BAND)

$$V_{TH0} = V_{FB} + 2\phi_F + \gamma \sqrt{2\phi_F}.$$

- V_{TH0} JE TEHNOLOŠKI PARAMETAR [ULAZNA I OBITA RAVNI POTENCIJAL METAL (POLY) - POLUPROVODNIK, POVRŠINSKA STANJA (TRAPOVI), PODEŠAVANJE NAPONA PRAGA (ENHANCEMENT MODE),...]
- EFEKAT "PODLOGE" (BODY-EFFECT) JE POVEĆANJE NAPONA PRAGA USLED POVEĆANJA NAPONA INVERZNE POLARIZACIJA PN SPOJA SORS - OSNOVA (BALK), V_{SB}.

$$V_{TH_1} \propto Q_d = S\sqrt{2 q \varepsilon N_A (2\phi_F)} \Rightarrow V_{TH_1} < V_{TH_2} \Rightarrow V_{TH_2} \propto Q_d = S\sqrt{2 q \varepsilon N_A (2\phi_F + V_{SB})}$$



$$V_{TH} = \underbrace{V_{FB} + 2\phi_F}_{V_{TH0}} + \gamma\sqrt{2\phi_F + V_{SB}} - \gamma\sqrt{2\phi_F} + \gamma\sqrt{2\phi_F} = V_{TH0} + \gamma\left[\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F}\right]$$

V_{TH0} – NAPON PRAGA KOJI UZIMA U OBZIR RAZLIKU POTENCIJALA IZMEĐU SORSA I OSTROVA.

γ – FAKTOR PODLOGE [BODY-FACTOR] TIPIČNO $0.4 \div 0.5\ V^{1/2}$.

PRIMER 6 TEHNOLOŠKI PROCES NUDI NMOS TRANZISTORE SA $V_{TH0_{NMOS}} = 0.32V$ I PMOS TRANZISTORE SA $V_{TH0_{PMOS}} = 0.3V$. ODREDITI RELATIVNU PROMENU NAPONA PRAGA AKO JE $V_{SB_{NMOS}} = V_{BS_{PMOS}} = 0.9V$, AKO JE $\gamma_{NMOS} = 0.4\ V^{1/2}$ I $\gamma_{PMOS} = 0.5^{1/2}$. UZETI $\phi_{F_{NMOS}} = 0.3V$ I $\phi_{F_{PMOS}} = 0.36\ V$. NAPON NAPAJANJA JE $V_{DD} = 1.8\ V$.

$$V_{TH_{NMOS}} = V_{TH0_{NMOS}} + \gamma_{NMOS}\left(\sqrt{2\phi_{F_{NMOS}} + V_{SB_{NMOS}}} - \sqrt{2\phi_F}\right) = 0.32 + 0.4\left(\sqrt{0.6+0.9} - \sqrt{0.6}\right) \approx 0.5V$$

$$V_{TH_{PMOS}} = V_{TH0_{PMOS}} + \gamma_{PMOS}\left(\sqrt{2\phi_{F_{PMOS}} + V_{BS_{PMOS}}} - \sqrt{2\phi_F}\right) = 0.30 + 0.5\left(\sqrt{0.72+0.9} - \sqrt{0.72}\right) \approx 0.512\ V$$

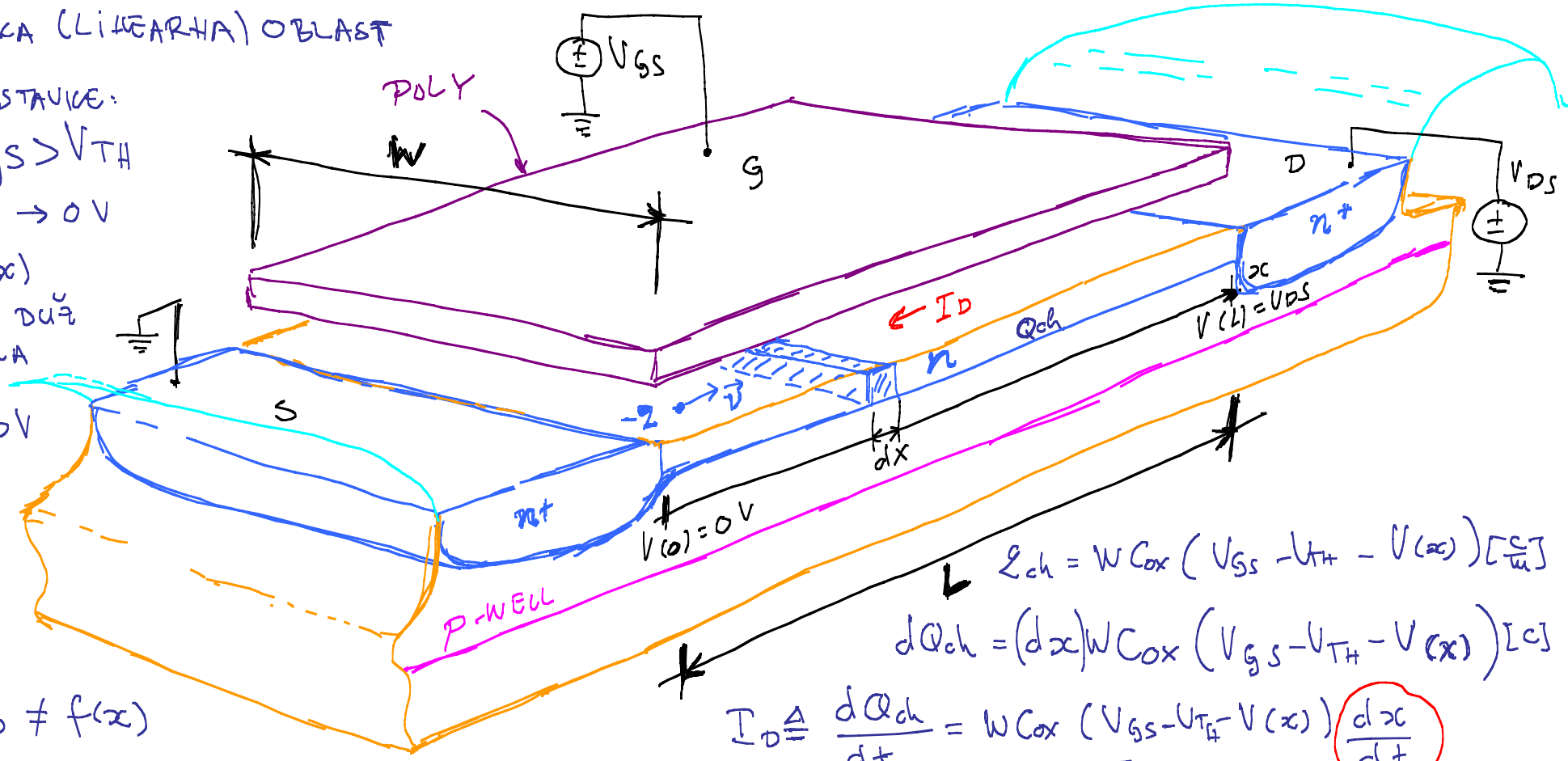
$$\delta V_{TH_{NMOS}} = \frac{|V_{TO_{NMOS}} - V_{TH_{NMOS}}|}{V_{TH0_{NMOS}}} = \frac{|0.32 - 0.5|}{0.32} = 0.563\ (56.3\ \%)$$

$$\delta V_{TH_{PMOS}} = \frac{|V_{TH0_{PMOS}} - V_{TH0_{PMOS}}|}{V_{TH0_{PMOS}}} = \frac{|0.3 - 0.512|}{0.3} = 0.707\ (70.7\ \%)$$

☐ OMSKA (LINEARNA) OBLAST

PREDPOSTAVKE:

- ▷ $V_{GS} > V_{TH}$
- ▷ $V_{DS} \to 0\ V$
- ▷ $V(x)$ NAPOTI DUŠ KANALA
- ▷ $V_{SB} = 0\ V$



- ▷ $I_D \neq f(x)$

$$\mathcal{Q}_{ch} = W C_{ox} \left(V_{GS} - V_{TH} - V(x) \right) \left[\frac{C}{m} \right]$$

$$dQ_{ch} = (dx) W C_{ox} \left(V_{GS} - V_{TH} - V(x) \right) [C]$$

$$I_D \triangleq \frac{dQ_{ch}}{dt} = W C_{ox} \left(V_{GS} - V_{TH} - V(x) \right) \frac{dx}{dt}$$

v [m/s]

$$E \triangleq -\frac{dV}{dx}, \quad v = -\mu_n E(x) \ [m/s], \quad v = \mu_n \frac{dV}{dx}, \quad I_D = W C_{ox} \left(V_{GS} - V_{TH} - V(x) \right) v$$

μ_n ↓ POKRETLJIVOST $\left[\frac{m^2}{V \cdot s} \right]$

$$I_D = W C_{ox} \left(V_{GS} - V_{TH} - V \right) \mu_n \frac{dV}{dx} \Rightarrow \int_0^L I_D \, dx = \int_0^{V_{DS}} W C_{ox} \mu_n \left(V_{GS} - V_{TH} - V \right) dV$$

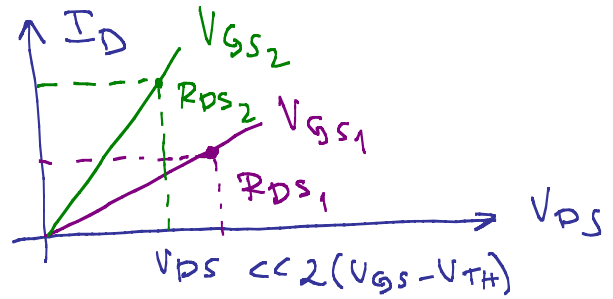
(A) $$I_D = \mu_n C_{ox} \frac{W}{L} \left[V_{DS} \left(V_{GS} - V_{TH} \right) - \frac{V_{DS}^2}{2} \right] = k_n \frac{W}{L} \left[V_{DS} \left(V_{GS} - V_{TH} \right) - \frac{V_{DS}^2}{2} \right]$$

$k_n = \mu_n C_{ox} = \mu_n \varepsilon_{ox} / t_{ox} \left[A/V^2 \right]$ → INTRINSIC TRANSISTOR GAIN, $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$

$\frac{V_{DS}^2}{2} \ll V_{DS}(V_{GS}-V_{TH}) \Rightarrow V_{DS} \ll 2(V_{GS}-V_{TH}) \Rightarrow I_D \approx \mu_n C_{ox} \frac{W}{L}(V_{GS}-V_{TH}) \cdot V_{DS} = R_{DS} V_{DS}$

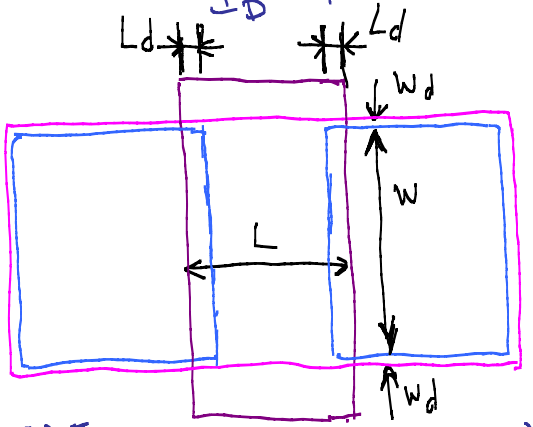
$R_{DS} = \frac{V_{DS}}{I_D} = \mu_n C_{ox} \frac{W}{L}(V_{GS}-V_{TH})$

OMSKA "LINEARNA" OBLAST →



$V_{GS_2} > V_{GS_1}$

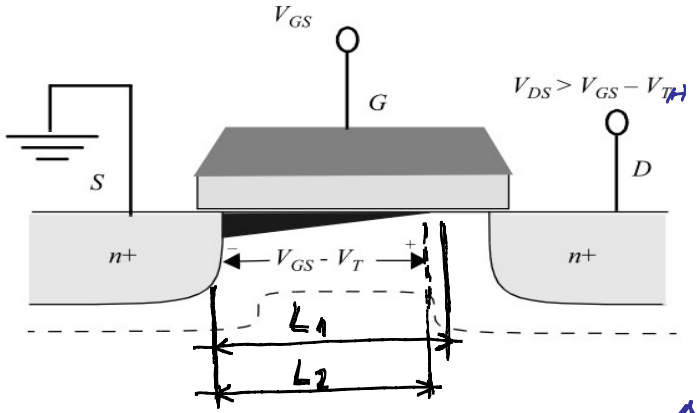
$R_{DS_2} < R_{DS_1}$



$L_{eff} = L - 2L_d = L - \Delta L$, $\Delta L = 2L_d$

$W_{eff} = W - 2W_d = L - \Delta W$, $\Delta W = 2W_d$

□ ZASIĆENJE ($V_{DS} \gg V_{TH}$)



$\int_0^L I_D = \int_0^{V_{DS}} \mu_n C_{ox} W [V_{GS}-V_T-V] dV$ i.e. $\frac{\partial I_D}{\partial V_{DS}} = 0$

$V_{DS} = V_{GS} - V_{TH}$

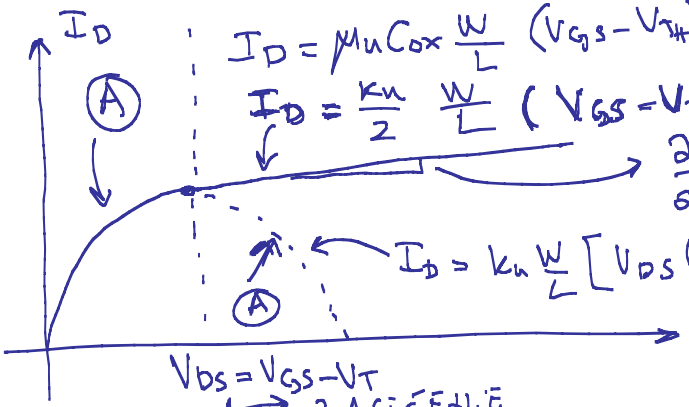
$V_{DS} = V_{GS} - V_{TH}$

$I_D = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS}-V_{TH})(V_{GS}-V_{TH}) - \frac{(V_{GS}-V_{TH})^2}{2}\right]$

$I_D = \frac{k_n}{2}\frac{W}{L}(V_{GS}-V_{TH})^2(1+\lambda V_{DS})$, $\lambda \approx 0.01\,V^{-1}$

$\frac{\partial I_D}{\partial V_{DS}} \approx \lambda I_D$ FAKTOR MODULACIJE DUŽINA KANALA.

$I_D = k_n \frac{W}{L}\left[V_{DS}(V_{GS}-V_{TH}) - \frac{V_{DS}^2}{2}\right]$

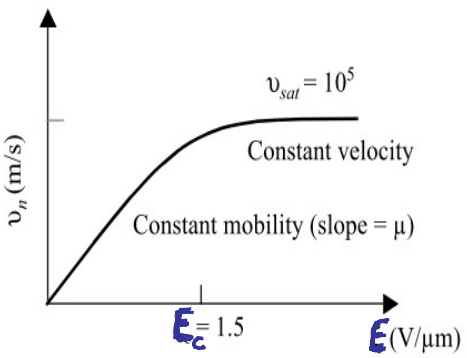


$L_2(V_{DS_2} > V_{DS_1}) < L_1(V_{DS_1}) \Rightarrow \lambda \propto \frac{\Delta L}{L}$

$Q_{ch} = W C_{ox}(V_{GS} - V_{TH} - V(x))$ [C/m]

$V(L) = V_{DS} = V_{GS} - V_{TH} \Rightarrow Q_{ch} = 0$ C/m KANAL SE PREKIDA NA STRANI DRENA. ["PINCH-OFF" EFEKAT]!

☐ ZASIĆENJE BRZINE NOSILACA NAELEKTRISANJA [VELOCITY SATURATION]



▷ NPR. ZA 130 nm PROCES GDE JE $V_{DD} = 1.8\,V$ i $L_{min} = 0.13\,\mu m$ KRITIČNO POLJE, E_c, SE POSTIŽE ODPRILIKE ZA $L_c \approx \frac{V_{DD}}{E_c} = \frac{1.8\,V}{1.5\,V/\mu m} = 1.2\,\mu m$ ŠTO JE OKO $10 L_{min}$!
ILUSTRATIVNO ZA $L_{min} = 0.13\,\mu m$ POLJE JE: $E \approx \frac{V_{DD}}{L_{min}} \approx 11.5\,V/\mu m$.

▷ ZA SUB-MIKRONSKE PROCESE SVI TRANZISTORI SU U REŽIMU ZASIĆENJA BRZINE NOSILACA NAELEKTRISANJA. $\left[v_{sat} \approx 10^5 \frac{m}{s} = 10^7 \frac{cm}{s}\right]$.

▷ MODEL PRVOG REDA

$$v = \begin{cases} \dfrac{\mu E}{1 + E/E_c}, & \text{ZA } E < E_c \\ v_{sat}, & \text{ZA } E \geq E_c \end{cases}$$

• GRANIČNI USLOV:

$$v(E_c) = v_{sat} = \frac{\mu E_c}{1 + E_c/E_c} = \frac{\mu E_c}{2} \Rightarrow E_c = \frac{2 v_{sat}}{\mu}$$

• PRETPOSTAVKE:

① FAKTOR $\frac{1}{1+E/E_c} \approx const$ ZA $V_{DS} \to 0\,V$.

② FAKTOR $\frac{1}{1+E/E_c}$ IMA UTICAJ SAMO ZA $V = V_{DS} \approx V_{DD}$ GDE SE POLJE MOŽE APROKSIMIRATI SA $E \approx \frac{V_{DS}}{L}$.
↑ NA PODU KANALA

③ $\lambda = 0\,V^{-1}$.

$$I_D = \frac{dQ_{ch}}{dt} = W C_{ox}(V_{GS} - V_{TH} - V)\frac{dx}{dt} = W C_{ox}(V_{GS} - V_{TH} - V)\left[\frac{-\mu_n E}{1 + E/E_c}\right]$$

$$\approx W C_{ox}(V_{GS} - V_{TH} - V)\frac{\mu_n}{1 + E/E_c}\frac{dV}{dx} \Rightarrow I_D(V_{GS}, V_{DS}) \approx \frac{\mu_n C_{ox}}{1 + V_{DS}/LE_c}\frac{W}{L}\left[V_{DS}(V_{GS} - V_{TH}) - \frac{V_{DS}^2}{2}\right] \quad (1)$$

- V_{DSAT} NAPON PREDNAPONA PRI KOJEM DOLAZI DO ZASIĆENJA BRZINE KRETANJA NOSILACA.
- I_{DSAT} STRUJA KOJA ODGOVARA V_{DSAT}.

$$I_D = \frac{dQ}{dt} = W C_{ox}(V_{GS} - V_{TH} - V)\frac{dx}{dt} = W C_{ox}(V_{GS} - V_{TH} - V)\, v_{sat} = W C_{ox} v_{sat}(V_{GS} - V_{TH} - V)$$

$$I_{DSAT} = I_D(V_{GS}, V = V_{DSAT}) = W C_{ox} v_{sat}(V_{GS} - V_{TH} - V_{DSAT}). \quad (2)$$

- V_{DSAT} SE DOBIJA IZJEDNAČAVANJEM (1) i (2) ZA $V_{DS} = V_{DSAT}$.

$$I_{DSAT} = I_D(V_{GS}, V_{DS} = V_{DSAT})$$

$$W C_{ox} v_{sat}\left[V_{GS} - V_{TH} - V_{DSAT}\right] = \frac{\mu_n C_{ox}}{1 + \frac{V_{DSAT}}{L E_c}} \frac{W}{L}\left[V_{DSAT}(V_{GS} - V_{TH}) - \frac{V_{DSAT}^2}{2}\right]$$

$$\cancel{W C_{ox}} \frac{\cancel{\mu_n} E_c}{2}\left[V_{GS} - V_{TH} - V_{DSAT}\right] = \frac{\cancel{\mu_n C_{ox}}}{1 + \frac{V_{DSAT}}{L E_c}} \frac{\cancel{W}}{\cancel{L}} V_{DSAT}\left[2(V_{GS} - V_{TH}) - V_{DSAT}\right]$$

$$\cancel{E_c}\left[V_{GS} - V_{TH} - V_{DSAT}\right] = \frac{\cancel{E_c} L V_{DSAT}}{E_c L + V_{DSAT}} \cdot \frac{1}{\cancel{L}}\left[2(V_{GS} - V_{TH}) - V_{DSAT}\right]$$

$$\left[E_c L + V_{DSAT}\right]\left[V_{GS} - V_{TH} - V_{DSAT}\right] = V_{DSAT}\left[2(V_{GS} - V_{TH}) - V_{DSAT}\right]$$

$$E_c L\left[V_{GS} - V_{TH} - V_{DSAT}\right] + \cancel{V_{DSAT}\left[V_{GS} - V_{TH}\right]} - \cancel{V_{DSAT}^2} = \cancel{2} V_{DSAT}(V_{GS} - V_{TH}) - \cancel{V_{DSAT}^2}$$

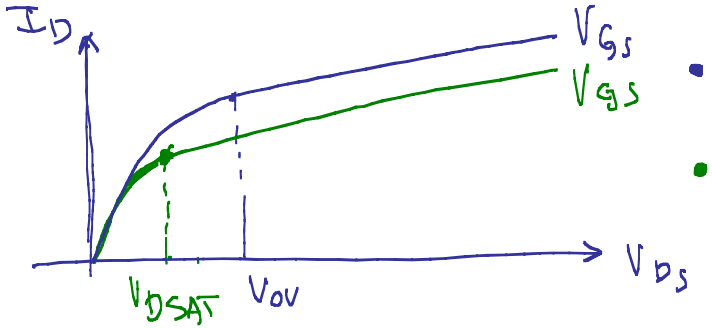
$$E_c L\left[V_{GS} - V_{TH}\right] = V_{DSAT}\left[(V_{GS} - V_{TH}) + E_c L\right]$$

$$V_{DSAT} = \frac{(V_{GS}-V_{TH})}{1+\frac{(V_{GS}-V_{TH})}{E_c L}} = \frac{V_{OV}}{1+\frac{V_{OV}}{E_c L}}, \quad V_{OV} = V_{GS}-V_{TH} \rightarrow \text{EFEKTIVNI NAPON } V_{GS}$$

[OVERDRIVE VOLTAGE.]

▷ ZA "KRATKO-KANALNE" TRANZISTORE ("SHORT-CHANNEL") I DOVOLJNO VELIKO V_{OV}

$$\frac{1}{1+V_{OV}/E_c L} < 1 \Rightarrow V_{DSAT} < V_{OV}.$$



- KLASIČNO ZASIĆENJE ("LONG CHANNEL")
- ZASIĆENJE BRZINE ("SHORT CHANNEL")

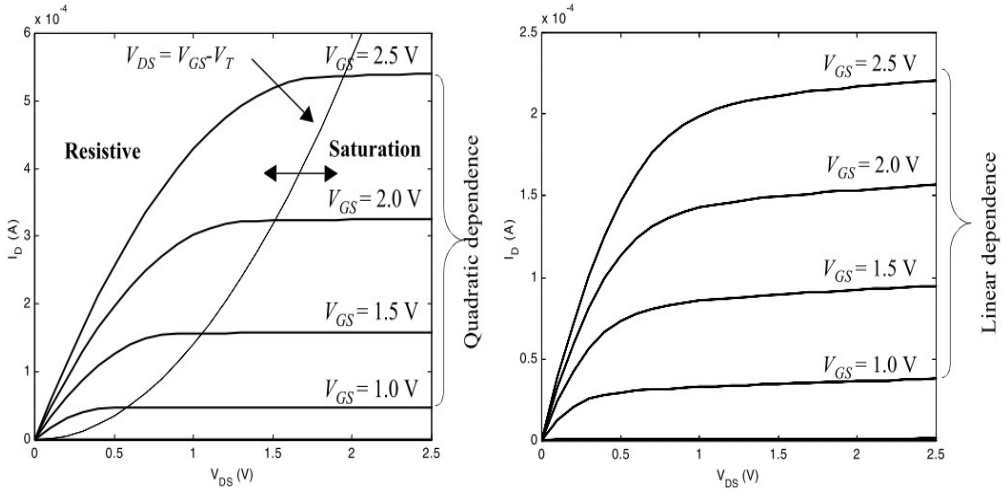
▷ ZA DOVOLJNO VELIKA POLJA I KRATAK KANAL MODEL SE MOŽE POJEDNOSTAVITI:

$$v = \begin{cases} \mu E, & \text{ZA } E \ll E_c \\ v_{sat}, & \text{ZA } E \gg E_c \end{cases}, \quad v_{sat} \approx \mu E_c, \quad V_{DSAT} = \frac{V_{OV}}{1+\frac{V_{OV}}{L E_c}} \approx L E_c \;\Big|\; \Rightarrow E_c = \frac{V_{DSAT}}{L}, \; \frac{V_{OV}}{L E_c} \gg 1$$

$$I_{DSAT} \equiv I_D(V_{GS}, V_{DS}=V_{DSAT}) = \mu_n C_{ox} \frac{W}{L}\left[V_{DSAT}V_{OV} - \frac{V_{DSAT}^2}{2}\right]$$

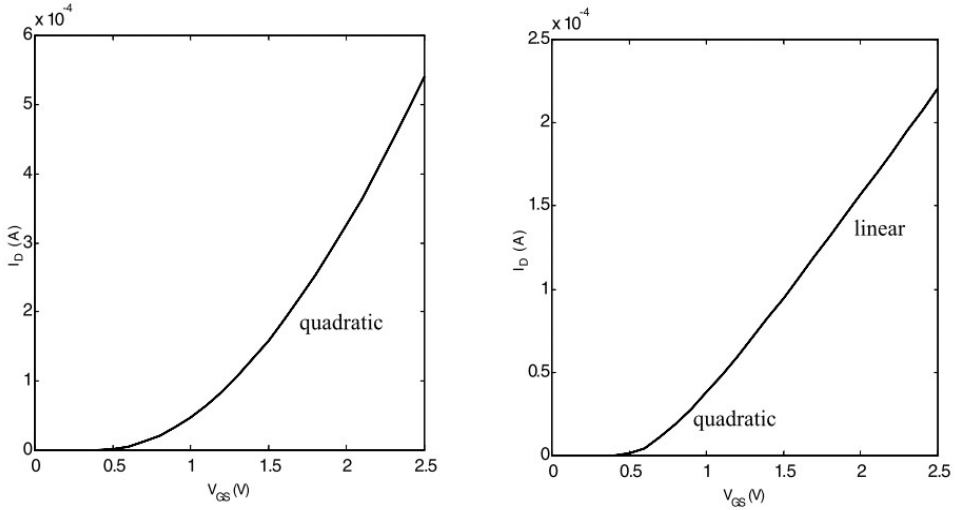
$$= W C_{ox} \mu_n \underbrace{\frac{V_{DSAT}}{L}}_{E_c}\left[V_{OV} - \frac{V_{DSAT}}{2}\right] = W C_{ox} \underbrace{\mu_n E_c}_{v_{sat}}\left[V_{OV} - \frac{V_{DSAT}}{2}\right] = W C_{ox} v_{sat}\left[V_{OV} - \frac{V_{DSAT}}{2}\right]$$

$$I_{DSAT} = W C_{ox} v_{sat}\left[V_{GS} - V_T - \frac{V_{DSAT}}{2}\right] \Rightarrow \text{STRUJA LINEARNA FUNKCIJA } V_{GS} \text{ ?}$$



(a) Long-channel transistor (L_d = 10 µm) (b) Short-channel transistor (L_d = 0.25 µm)

Figure 3.19 *I-V* characteristics of long- and a short-channel NMOS transistors in a 0.25 µm CMOS technology. The (*W*/*L*) ration of both transistors is identical and equals 1.5



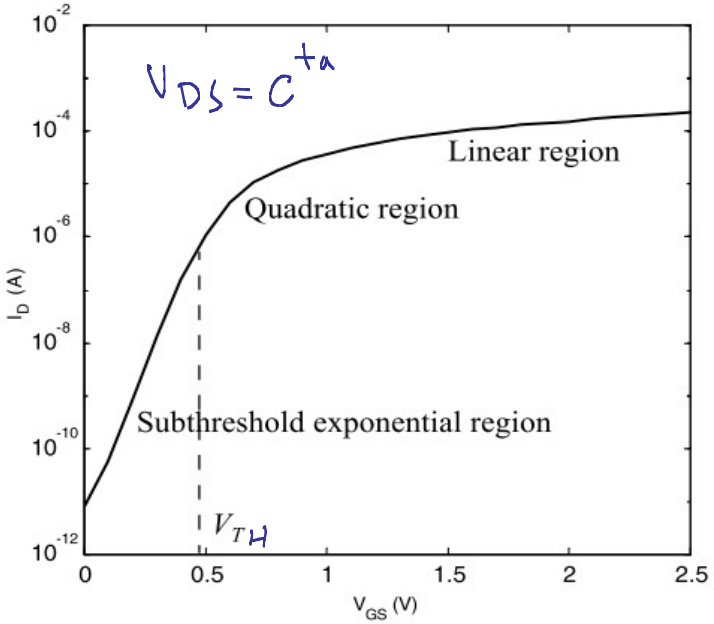
(a) Long-channel device (L_d = 10 µm) (b) Short-channel device (L_d = 0.25 µm)

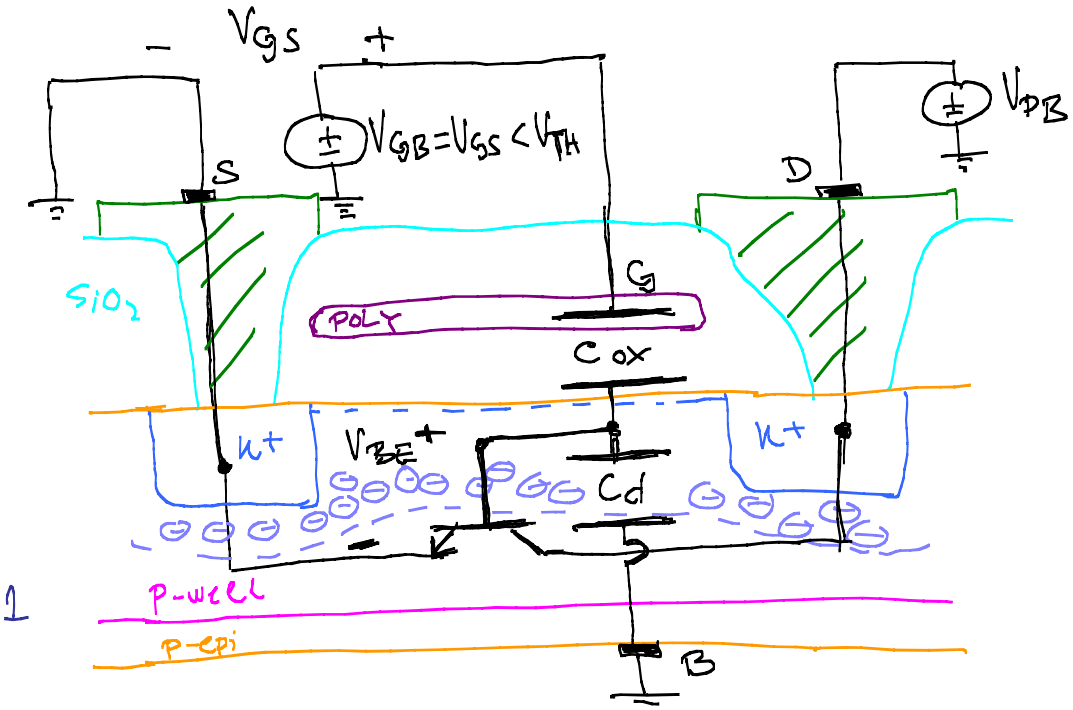
Figure 3.20 NMOS transistor I_D-V_{GS} characteristic for long and short-channel devices (0.25 µm CMOS technology). W/L = 1.5 for both transistors and V_{DS} = 2.5 V.

PODPRAGOVSKI REŽIM RADA [SUB-THRESHOLD CONDUCTION]

ZA $V_{GS} < V_T$, $I_D \neq 0\,A$

$$I_D = I_{DS} e^{\frac{V_{GS}}{n V_T}} \left[1 - e^{-\frac{V_{DS}}{V_T}}\right], \quad V_T = \frac{kT}{q}$$





PRETPOSTAVKA: $V_{DS} \gg V_T \Rightarrow 1 - \frac{1}{e^{V_{DS}/V_T}} \approx 1$

$$g_{m_{MOS}} = \frac{\partial I_D}{\partial V_{GS}} = \frac{\partial}{\partial V_{GS}}\left[I_{DS} e^{\frac{V_{GS}}{n V_T}}\right]$$

$$= \frac{I_{DS}}{n V_T} e^{V_{GS}/nV_T} = \frac{I_D}{nV_T} < g_{m_{BJT}} = \frac{I_C}{V_T}$$

Tipično $n \approx 1.5 = 3/2$

EFEKTIVNI NAPON "BAZA-EMITOR" POD-PRAGOVSKOG BJT-a JE V_{GS} I UVEK JE MANJI OD V_{BE} STANDARDOG BJT-a [KAPACITIVNI RAZDELNIK]

$$V_{BE} = \frac{C_{ox}}{C_{ox} + C_d} V_{GS} = \frac{1}{1 + \frac{C_d}{C_{ox}}} V_{GS} = \frac{V_{GS}}{n}$$

$n = 1 + C_d/C_{ox}$, OBIČNO VAŽI $C_d < C_{ox}$.

- ZA RAZLIKU OD ANALOGNIH IC, U DIGITALNIM IC PODRAGOVSKI REŽIM PREDSTAVLJA PARAZITNI EFEKAT [POVEĆAVA STATIČKU SNAGU DISIPACIJE].

- DEGRADACIJA POKRETLJIVOSTI NOSILACA $\mu_{n,p}$
  - ZA MALE DEBLJINE OKSIDA, DO SADA ZANEMARIVANO, VERTIKALNO POLJE ($E_{VERT} \propto V_{GS}/t_{ox}$) DOLAZI DO IZRAŽAJA.
  - E_{VERT} UTIČE NA POKRETLJIVOST NOSILACA UGL. TAKO ŠTO JE REDUKUJE.

$$\text{EFEKTIVNA POKRETLJIVOST} \leftarrow \mu_{n,eff} = \frac{\mu_{n0}}{1+\eta(V_{GS}-V_{TH})}$$

μ_{n0} → POKRETLJIVOST BEZ UTICAJA E_{VERT}

η ← TEHNOLOŠKI PARAMETAR [EMPIRIJSKI SE ODREĐUJE].

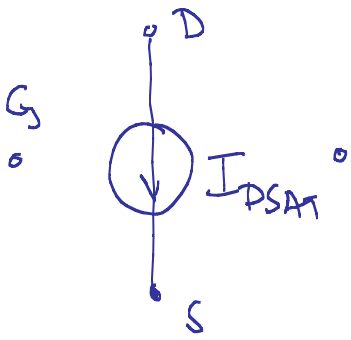
PRIMER 7 Koliko iznosi relativno umanjenje pokretljivosti elektrona usled vertikalnog polja je tranzistor polarisan sa $V_{OV} = 0.5V$ za tehnološki proces koji ima $\eta = 0.1V^{-1}$, za pokretljivost elektrona bez uticaja vertikalnog polja uzeti $\mu_{n0} = 1200 \frac{cm^2}{V \cdot s}$.

$$V_{GS} - V_{TH} = V_{OV} = 0.5V, \quad \mu_{n,eff} = \frac{\mu_0}{1+\eta V_{OV}} = \frac{1200\ cm^2/V\cdot s}{1 + 0.1V^{-1} \times 0.1V} \approx 1143\ cm^2/V\cdot s$$

$$\delta\mu_n = \frac{|\mu_{no} - \mu_{n,eff}|}{\mu_{no}} = \frac{57\ cm^2/V.s}{1200\ cm^2/V.s} = 0.0475 \quad (4.75\ \%)$$

GENERALIZOVANI (POJEDNOSTAVLJENI) MODEL MOS-FETa U DIGITALNIM IC ZA SUB-MIKRONSKE PROCESE

nMOS



$$I_D = \begin{cases} 0, & V_{GS} < V_{TH} \\ k_n \frac{W}{L} V_{Min} \left[V_{OV} - \frac{V_{Min}^2}{2} \right] \left[1 + \lambda V_{DS} \right], & V_{GS} \geq V_{TH} \end{cases}$$

$$V_{Min} = \min \left\{ V_{DSAT}, V_{DS}, V_{OV} \right\}$$

$$V_{OV} = V_{GS} - V_{TH}$$

$$V_{TH} = V_{THO} + \gamma \left[\sqrt{2\Phi_F + V_{SB}} - \sqrt{2\Phi_F} \right], \quad \gamma \approx 0.4\sqrt{V}, \quad \Phi_F \approx 0.3\ V$$

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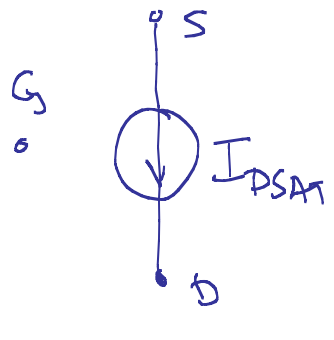
pMOS



$$I_D = \begin{cases} 0, & V_{SG} < V_{TH} \\ k_n \frac{W}{L} V_{Min} \left[V_{OV} - \frac{V_{Min}^2}{2} \right] \left[1 + \lambda V_{SD} \right], & V_{SG} \geq V_{TH} \end{cases}$$

$$V_{Min} = \min \left\{ V_{DSAT}, V_{SD}, V_{OV} \right\}$$

$$V_{OV} = V_{SG} - V_{TH}$$

$$V_{TH} = V_{THO} + \gamma \left[\sqrt{2\Phi_F + V_{SB}} - \sqrt{2\Phi_F} \right], \quad \gamma \approx 0.5\sqrt{V}, \quad \Phi_F \approx 0.35\ V$$

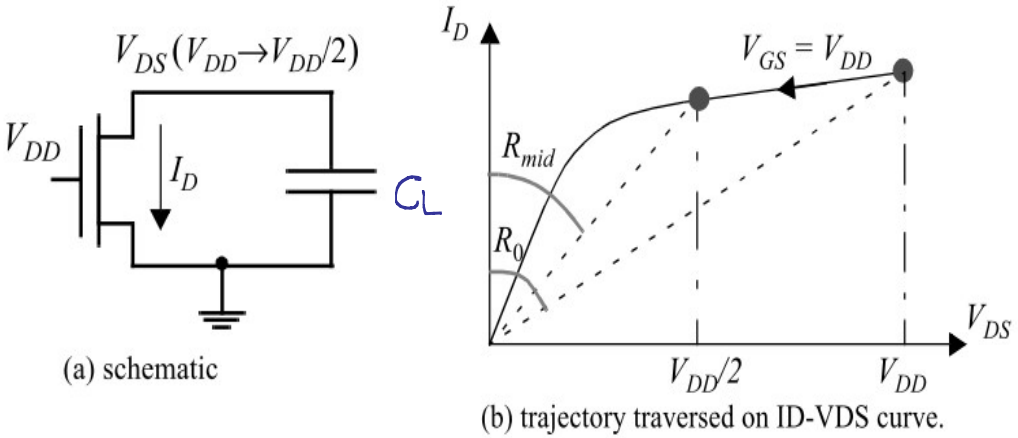
☐ EKVIVALENTNA OTPORNOST KANALA MOS-FET-a U DIGITALNIM IC ZA VELIKE SIGNALE.

DINAMIČKA NELINEARNA OTPORNOST

$$R_c = f(V_{GS}, V_{DS}, V_{TH}, W, L, PUT, \dots)$$

$$R_{cav} = \frac{1}{t_2 - t_1}\int_{t_1}^{t_2} \frac{v_{DS}(t)}{i_D(t)}\,dt$$

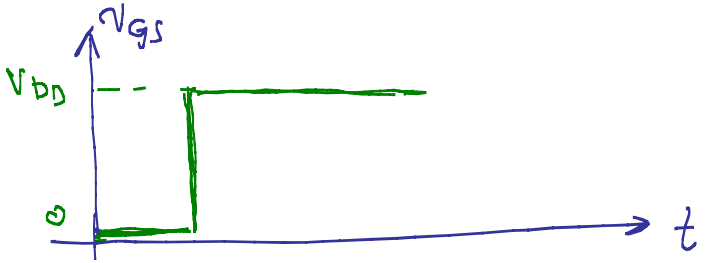
$$\approx \frac{1}{2}\left[R_c(t_1) + R_c(t_2)\right]$$

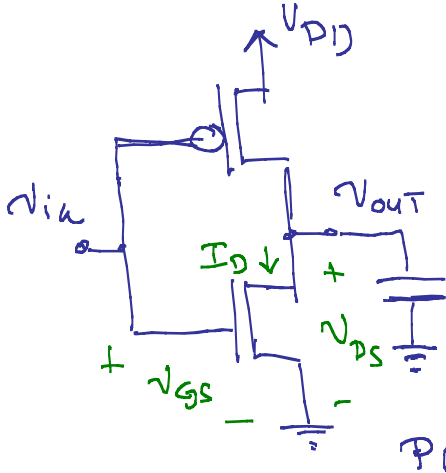


(a) schematic

(b) trajectory traversed on ID-VDS curve.

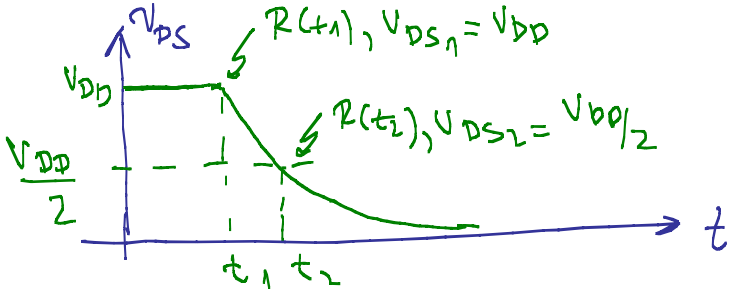
$$R_{cav} = \frac{1}{V_{DS_2} - V_{DS_1}}\int_{V_{DS_1}}^{V_{DS_2}} \frac{V}{I_{DSAT}(1+\lambda V)}\,dV$$





$$I_{DSAT} = k_n \frac{W}{L} V_{DSAT}\left(V_{OV} - \frac{V_{DSAT}}{2}\right)$$

$$k_n = \mu_n C_{ox}$$



$V_{DS_1} = V_{DD}$, $V_{DS_2} = V_{DD}/2$

PRETPOSTAVKA: $\lambda V \ll 1 \Rightarrow \frac{1}{1+\lambda V} \approx 1 - \lambda V$

$$R_{cav} = \frac{1}{-\frac{V_{DD}}{2}}\int_{V_{DD}}^{V_{DD/2}} \frac{V}{I_{DSAT}}(1-\lambda V)\,dV = \frac{2}{V_{DD} I_{DSAT}}\left[\int_{V_{DD/2}}^{V_{DD}} V\,dV - \lambda\int_{V_{DD/2}}^{V_{DD}} V^2\,dV\right] = \frac{2}{V_{DD} I_{DSAT}}\left[\frac{V^2}{2}\Big|_{V_{DD/2}}^{V_{DD}} - \lambda\frac{V^3}{3}\Big|_{V_{DD/2}}^{V_{DD}}\right]$$

$$R_{eqv} = \frac{2}{V_{DD} I_{DSAT}} \left[\frac{1}{2}\left(V_{DD}^2 - \frac{V_{DD}^2}{4}\right) - \lambda \frac{1}{3}\left(V_{DD}^3 - \frac{V_{DD}^3}{8}\right) \right] = \frac{V_{DD}}{I_{DSAT}} \left[\frac{3}{4} - \lambda \frac{2}{3} \frac{7}{8} V_{DD} \right]$$

$$R_{eqv} \approx \frac{3}{4} \frac{V_{DD}}{I_{DSAT}} \left[1 - \frac{7}{9} \lambda V_{DD} \right]$$

PROSTIM USREDNJAVANJEM SE DOBIJA:

$$R'_{eqv} = \frac{1}{2} \left[\frac{V_{DD}}{I_{DSAT}(1+\lambda V_{DD})} + \frac{V_{DD}/2}{I_{DSAT}(1+\lambda V_{DD}/2)} \right] \approx \frac{1}{2} \frac{V_{DD}}{I_{DSAT}} \left[1 - \lambda V_{DD} + \frac{1}{2} - \lambda \frac{V_{DD}}{4} \right]$$

$$R'_{eqv} \approx \frac{1}{2} \frac{V_{DD}}{I_{DSAT}} \left[\frac{3}{2} - \frac{5}{4} \lambda V_{DD} \right] = \frac{3}{4} \frac{V_{DD}}{I_{DSAT}} \left[1 - \frac{5}{6} \lambda V_{DD} \right] \approx R_{eqv}$$

- U DIGITALNIM IC, $L = L_{min}$. PA SE ZA VEĆU ŠIRINU KANALA (W) DOBIJA SE MANJA OTPORNOST

$$I_{DSAT} \propto \left(\frac{W}{L}\right) \Rightarrow R_{eqv} \propto 1/(W/L) \Rightarrow (W/L) \uparrow \Rightarrow R_{eqv} \downarrow$$

- ZA $V_{DD} \gg V_{TH} + V_{DSAT}/2$, OTPORNOST KANALA GOTOVO DA NE ZAVISI OD NAPONA NAPAJANJA (V_{DD}):

$$I_D = k_n \frac{W}{L} V_{DSAT} \left(V_{OV} - \frac{V_{DSAT}}{2} \right), \quad V_{GS} = V_{DD}, \quad V_{OV} - \frac{V_{DSAT}}{2} = V_{DD} - \left(V_{TH} + \frac{V_{DSAT}}{2} \right)$$

ZA $V_{DD} \gg V_{TH} + V_{DSAT}/2 \Rightarrow I_{DSAT} \approx k_n \frac{W}{L} V_{DSAT} V_{DD}$ I $\lambda \to 0\ V^{-1}$:

$$R_{eqv} \approx \frac{3}{4} \frac{V_{DD}}{k_n \frac{W}{L} V_{DD} V_{DSAT}} \Bigg|_{\lambda \to 0\ V^{-1}} = \frac{3}{4} \left(\frac{L}{W}\right) \frac{1}{k_n V_{DSAT}} \Rightarrow R_{eqv} \neq f(V_{DD})$$

▷ ZA $V_{DD} \approx V_{TH}$ OTPORNOST KANALA NAGLO RASTE

$$|I_{DSAT}| = k_n \frac{W}{L} V_{DSAT} \left| V_{DD} - V_{TH} - \frac{V_{DSAT}}{2} \right| \approx k_n \frac{W}{L} \frac{V_{DSAT}^2}{2} \Rightarrow R_{cav} \approx \frac{3}{4} \frac{V_{DD}}{|I_{DSAT}|}$$

$V_{DD} \to V_{TH}$; $V_{DD} \to V_{TH}$; $\lambda \to 0\ V^{-1}$

$$R_{cav}(V_{DD} \approx V_{TH}) \approx \frac{3}{4}\left(\frac{L}{W}\right)\frac{1}{k_n V_{DSAT}}\left(\frac{V_{TH}}{V_{DSAT}}\right) > R_{cav}(V_{DD} \gg V_{TH} + V_{DSAT}/2)\left(\frac{V_{TH}}{V_{DSAT}}\right) > R_{cav}\left(V_{DD} \gg V_{TH} + \frac{V_{DSAT}}{2}\right)$$

$V_{TH} > V_{DSAT}$

$R_{cav}(V_{DD} \gg V_{TH} + V_{DSAT}/2)$

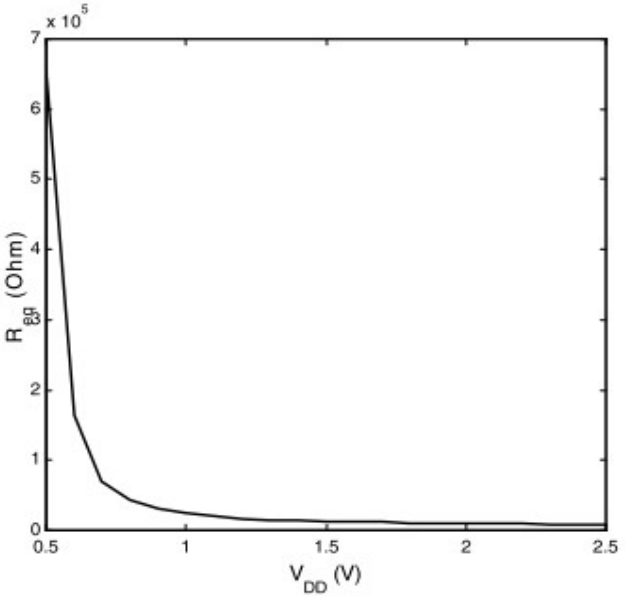


Table 3.3 Equivalent resistance R_{eq} ($W/L = 1$) of NMOS and PMOS transistors in 0.25 µm CMOS process (with $L = L_{min}$). For larger devices, divide R_{eq} by W/L.

↙ $V_{DD_{MAX}}$

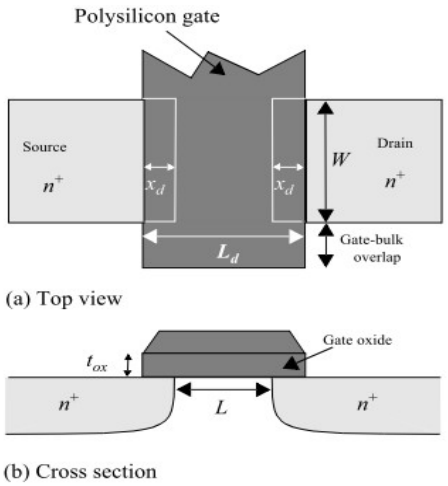
V_{DD} (V)	1	1.5	2	2.5
NMOS (kΩ)	35	19	15	13
PMOS (kΩ)	115	55	38	31

ZA ANALIZU PRVOG REDA INTERESANTNE SU VREDNOSTI R_{cav} U U OPSEGU $[V_{DD_{MAX}}/2, V_{DD_{MAX}}]$. (REDA DESETINA kΩ).

☐ DINAMIČKE KARAKTERISTIKE MOSFETa

ODREĐENE PARAZITNIM KAPACITIVNOSTIMA MOS STRUKTURE

D KAPACITIVNOST PREKLAPANJA [OVERLAP CAPACITANCE]



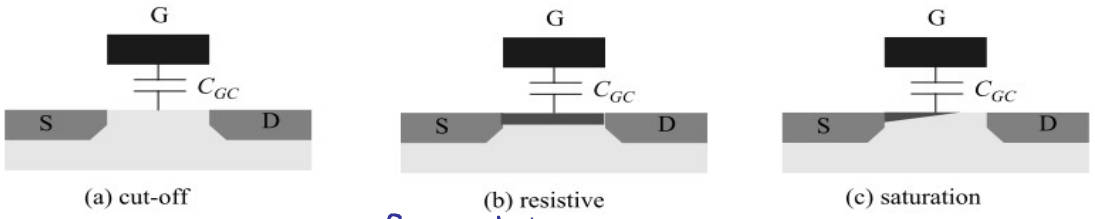
$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \; ; \; t_{ox} \approx \frac{L_{min}}{50}$$

PODUŽNA KAPACITIVNOST $\left[\frac{F}{m}\right]$

$$C_{GSO} = C_{GDO} = W \cdot x_d \cdot C_{ox} = W \cdot C_0'$$

- x_d i C_0' SU TEHNOLOŠKI PARAMETRI.

D KAPACITIVNOST KANALA [CHANNEL CAPACITANCE]



(a) $V_{GS} < V_{TH}$

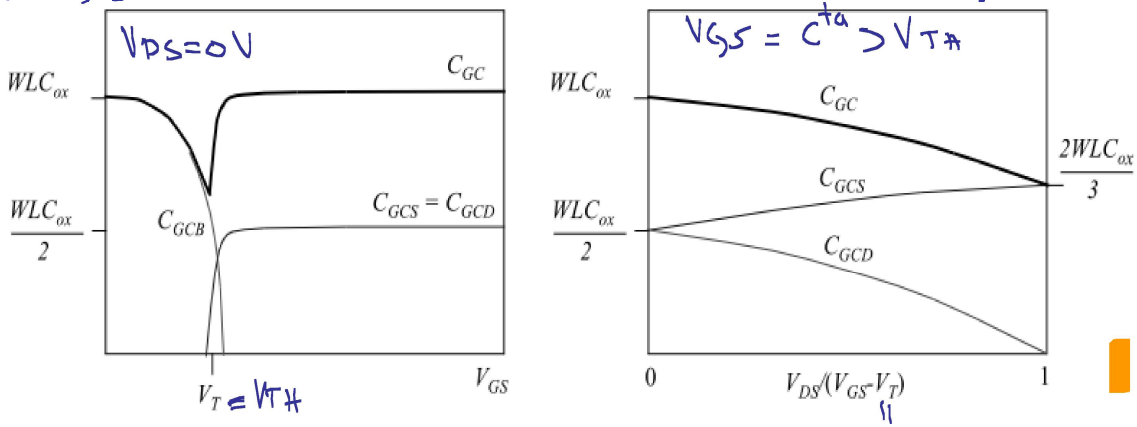
(b) $V_{DS} << 2(V_{GS} - V_{TH}) = 2V_{OV}$

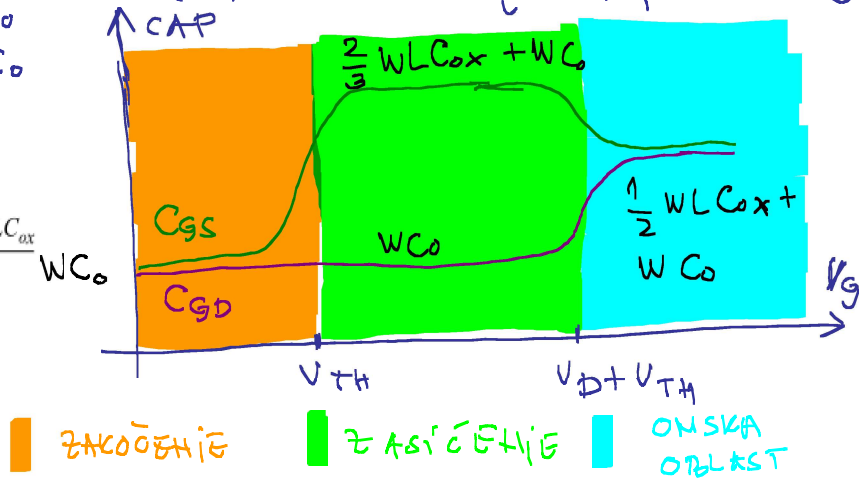
(c) $V_{DS} > \min\{V_{DSAT}, V_{GS} - V_{TH}\}$

$C_{GC} = C_{GCB} = WLC_{ox}$ $C_{GCD} = C_{GCS} = WC_0$

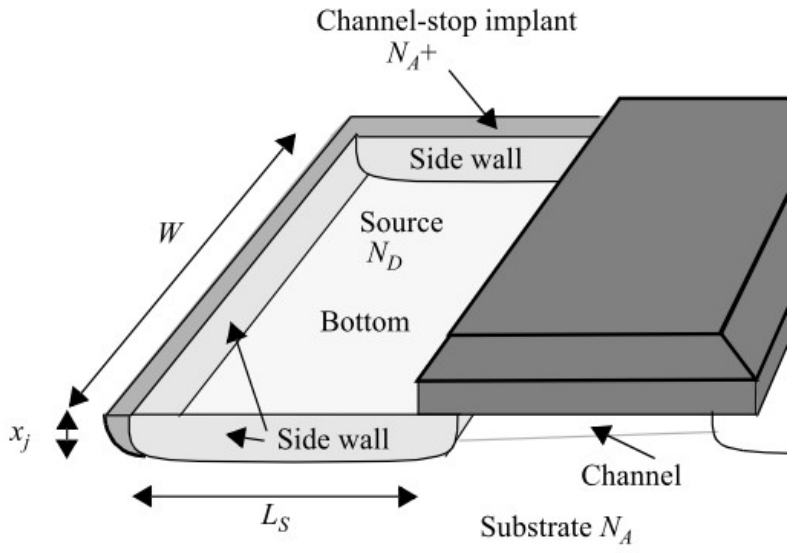
$C_{GCD} = C_{GCS} = \frac{WLC_{ox}}{2} + WC_0$ $C_{GCB} = 0F$

$C_{GCS} = \frac{2}{3}WLC_{ox} + WC_0$ $C_{GCD} = WC_0$

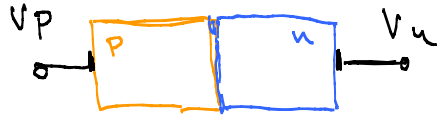




▷ KAPACITIVNOSTI PN SPOJA



$$\hat{C}_j = \frac{\hat{C}_{j0}}{\left(1 + \frac{V_R}{V_0}\right)^{m_j}} \quad ; \; V = V_P - U_{t1} \; ; \; V_R = V_H - V_P = -V$$



$\hat{C}_j$ [F/m²] POVRŠINSKA KAPACITIVNOST

$$V_R = \begin{cases} V_{SB}, V_{DB} & \text{ZA NMOS} \\ V_{BS}, V_{BD} & \text{ZA PMOS} \end{cases}$$

- UKUPNA KAPACITIVNOST SPOJEVA, C_j

$$C_j = C_{jBP} + C_{jsw} = W \cdot L_S \hat{C}_j + (W + 2L_S)\hat{C}_{jsw}$$

- DONJA PLOČA [BOTTOM-PLATE]

$$C_{jBP} = W \cdot L_S \hat{C}_j \; , \quad m_j = 0.5$$

- KAPACITIVNOST "ZIDOVA" [SIDE-WALL]

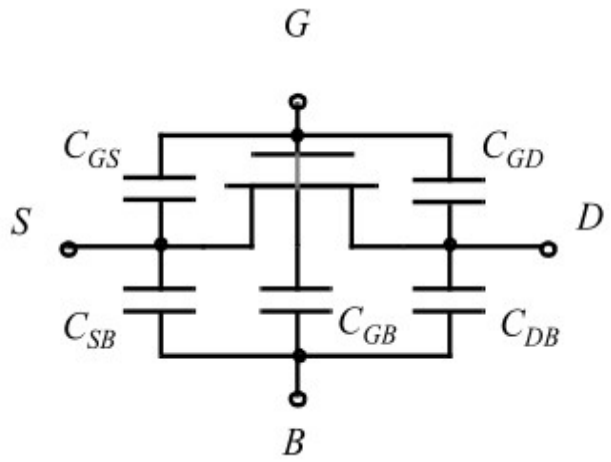
$$C_{jsw} = (W + 2L_S) \cdot x_j \hat{C}_j = (W + 2L_S)\hat{C}_{jsw} \; ,$$

$m_j = 1/3 \div 1/2$ $\quad \hat{C}_{jsw} = \hat{C}_j x_j$ [F/m]

↳ PODUŽNA KAPACITIVNOST.

KAPACITIVNOST ZIDA PREMA KANALU NAJČEŠĆE MOŽE DA SE ZANEMARI POŠTO SE RADI O SPOJU ISTOG TIPA POLUPROVODNIKA SA RELATIVNO MALOM RAZLIKOM U KONCENTRACIJAMA PRIMESA [PREKLOPNI - KANAL] TAKO DA OSIROMAŠENE OBLASTI GOTOVO DA I NEMA.

D MODEL MOS-FETa SA PARAZITNIM KAPACITIVNOSTIMA.



$$C_{GS} = C_{GCS} + C_{GSO} \quad (C_{GCS}: \text{CHANNEL}, \; C_{GSO}: \text{OVERLAP})$$

$$C_{GD} = C_{GCS} + C_{GSO}$$

$$C_{GB} = C_{GCB}$$

$$C_{SB} = C_{jS}, \quad C_{DB} = C_{jD} \quad (C_j: \text{JUNCTION})$$

PROJEKTANT IC KOLA KOJI ŽELI DA PROJEKTUJE KOLA VISOKIH PERFORMANSI I NISKE POTROŠNJE [LOW-POWER] TREBA DA RAZVIJE OSEĆAJ ZA RELATIVNI ODNOS I RED VELIČINE PARAZITNIH KAPACITIVNOSTI MOS-FETa.

PRIMER 8 MOS-FET IMA SLEDEĆE PARAMETRE: $t_{ox} = 8\,nm$, $L = 0.26\,\mu m$, $W = 1\,\mu m$, $L_S = 0.52\,\mu m$, $C_o' = 5\times10^{-10}\,F/m$, $C_{j0} = 10^{-3}\,F/m^2$, $C_{jsw} = 3\times10^{-10}\,F/m$.

ODREDITI SVE PARAZITNE KAPACITIVNOSTI PRI NULTOM NAPONU NAPAJANJA.

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \approx \frac{4\cdot\varepsilon_0}{t_{ox}} = \frac{4\cdot 8.85\times10^{-12}\,F/m}{8\,nm} = 4.314\times10^{-3}\,\frac{F}{m^2} = 4.314\,\frac{fF}{\mu m^2}$$

$$C_{GSO} = C_{GDO} = WC_o' = 0.5\,fF$$

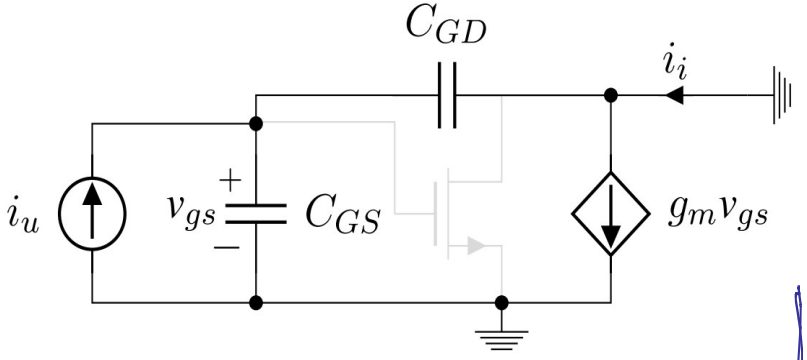
$$C_{GC} = C_{GCB} + C_{GCS} + C_{GCD} = C_{GCB} + C_{GSO} + C_{GDO} = C_{GCB} + 2WC_O'$$

$$C_{GC} = WL\,C_{ox} + 2\cdot W\cdot C_O' = (1\mu m \times 0.26\mu m)\,4.314\times10^{-3}\frac{F}{m^2} + 2\times1\mu m\times5\times10^{-10}\frac{F}{m} = 2.12\ fF$$

$$C_{SB} = C_{DB} = W\cdot L_S\cdot\hat{C}_{j0} + (W+2L_S)\,\hat{C}_{jsw}$$

$$= (1\mu m\times 0.52\mu m)\times10^{-3}\frac{F}{m^2} + (1\mu m + 2\times0.52\mu m)\cdot3\times10^{-10}\frac{F}{m} = 1.13\ fF$$

TRANZICIJSKA FREKVENCIJA, f_T



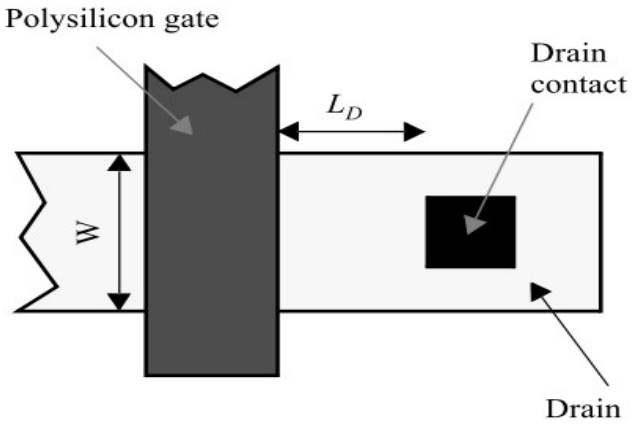
- PRETPOSTAVKA: U TAKVIM SLUČAJEVIMA $C_{GD} \ll C_{GS}$. PA SE MOŽE UZETI $C_{GD} \to 0F$.
- f_T JE FREKVENCIJA PRI KOJOJ MODUO STRUJNOG POJAČANJA PADNE NA 1.

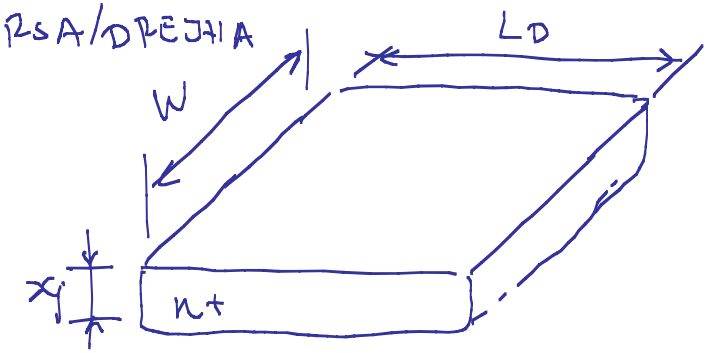
$$\left|\frac{i_i}{i_u}\right| \approx \frac{g_m}{\omega C_{GS}} = 1 \quad @\ \omega = \omega_T = 2\pi f_T$$

$$f_T = \frac{1}{2\pi}\frac{g_m}{C_{GS}} \approx \frac{1}{2\pi}\cdot\frac{\mu_n C_{ox}\frac{W}{L}V_{OV}}{\frac{2}{3}WLC_{ox}} = \frac{3}{4}\frac{\mu_n V_{OV}}{\pi\cdot L^2}$$

⇒ 2X MANJE L DAJE PRIBLIŽNO 4X BRŽI TRANZISTOR

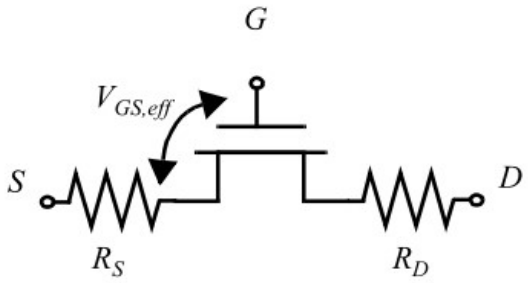
▷ EKVIVALENTNA OTPORNOST SORSA/DRejNA





OTPORNOST KONTAKTA

$$R_{S,D} = \rho \cdot \frac{L_{S,D}}{W \cdot x_j} + R_C = \frac{\rho}{x_j} \cdot \frac{L_{S,D}}{W} + R_C$$



$$R_{S,D} = R_\square \frac{L_{S,D}}{W} + R_C, \quad R_\square = \frac{\rho}{x_j} \left[\Omega/\square\right]$$

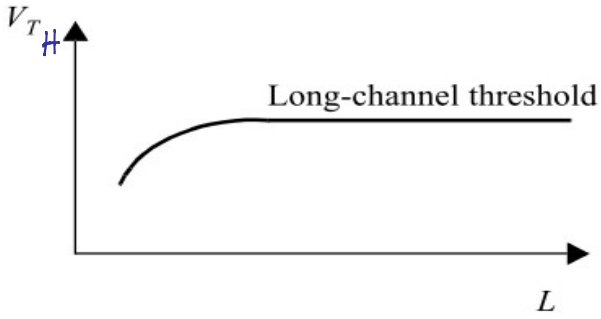
- $R_\square = 20 \div 100\ \Omega/\square$ BEZ SILICIDOM, SA SILICIDOM $R_\square = 1 \div 5\ \Omega/\square$.

□ EFEKTI DRUGOG REDA

▷ VARIJACIJA NAPONA PRAGA

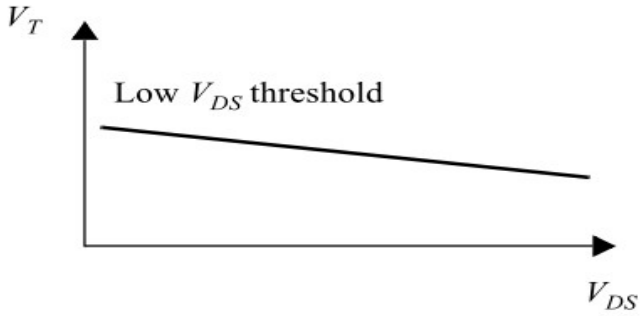
- LIBL - LENGTH INDUCED BARIER LOWERING
- DIBL - DRAIN INDUCED BARIER LOWERING

LiBL

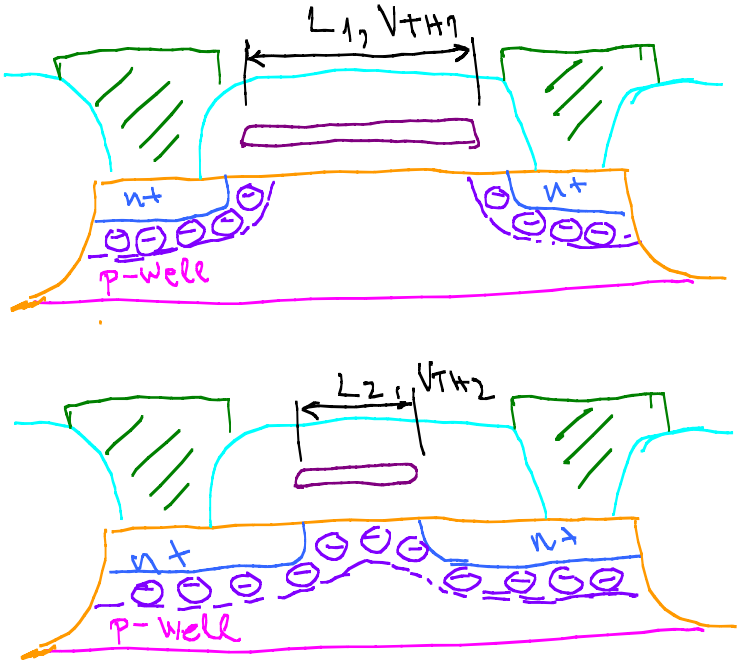


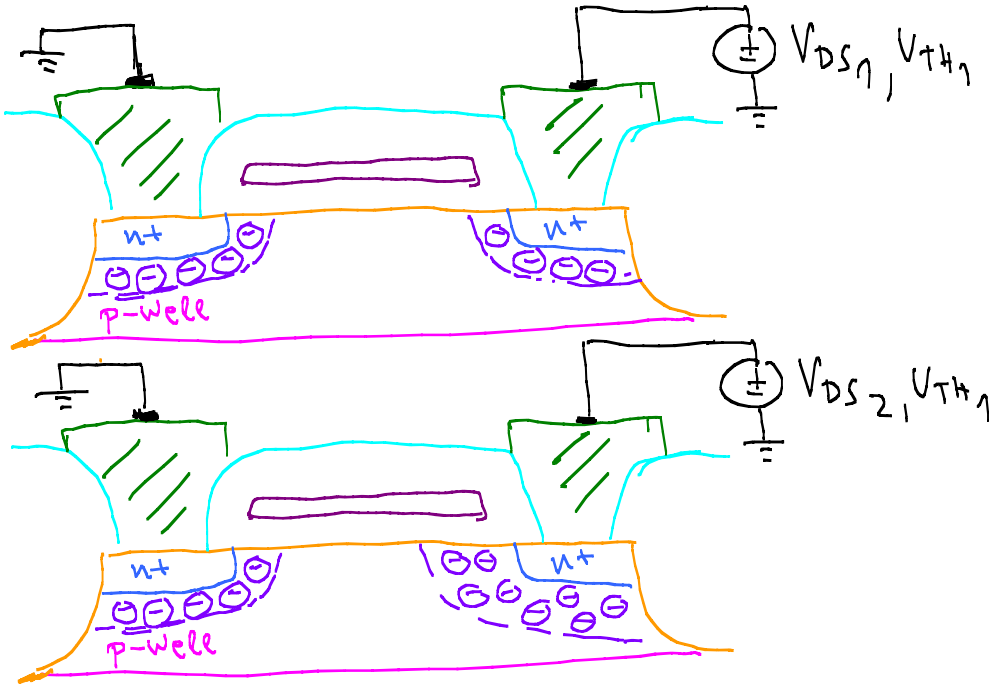
(a) Threshold as a function of the length (for low V_{DS})

DiBL



(b) Drain-induced barrier lowering (for low L)





(a) $L_1 > L_2 \Rightarrow V_{TH1} > V_{TH2}$

(b) $V_{DS1} < V_{DS2} \Rightarrow V_{TH1} > V_{TH2}$

(a) ZA KRATAK KANAL VEĆ POSTOJI OSIROMAŠENA OBLAST U OBLASTI KANALA KOJA POTIČE OD SPOJA DREJN (SORS) - BALK TAKO DA SE SA MANJIM NAPONOM PRAGA POSTIŽE INVERZIJA POVRŠINE.

(b) ZA VEĆI NAPON V_{DS} [INVERZNI NAPON ZA SPOJ DREJN - BALK] OSIROMAŠENA OBLAST SE ŠIRI KA PODRUČJU KANALA [BALK MANJE DOPIRAN OD DREJNA] PA JE POTREBAN MANJI NAPON PRAGA DA BI SE OSTVARILA INVERZIJA POVRŠINE.

D EFEKAT "VRUĆIH" NOSILACA [HCE - HOT-CARRIERS EFFECT]

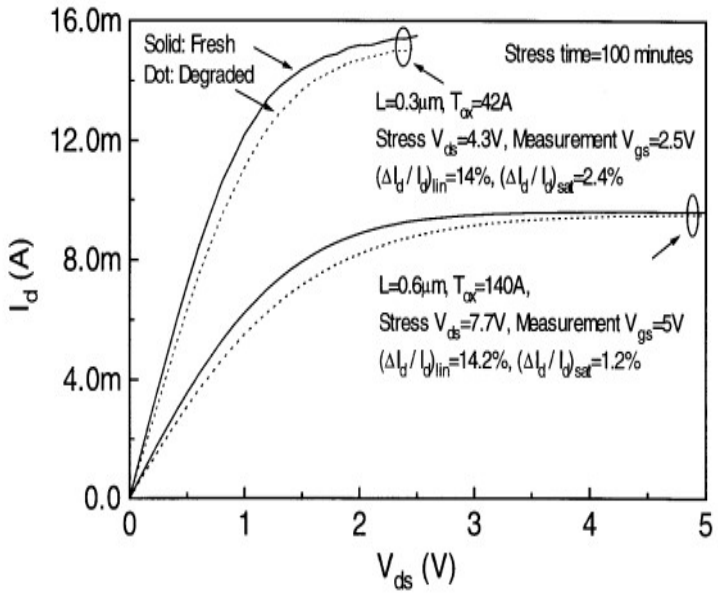
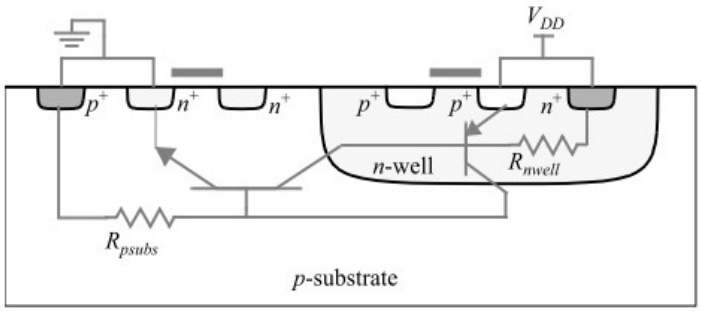


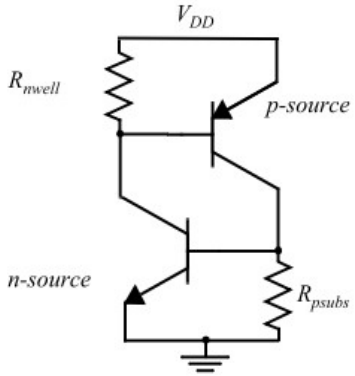
Figure 3.36 Hot-carrier effects cause the *I-V* characteristics of an NMOS transistor to degrade from extensive usage (from [McGaughy98]).

- USLED JAKOG ELEKTRIČNOG POLJA ($E \approx 10^4$ V/μm) DOLAZI DO NAGLOG PORASTA BRZINE KRETANJA NOSILACA KOJI MOGU DA STIČU DOVOLJNO VELIKU KINETIČKU ENERGIJU I TUNELOVATI U OKSID ["VRUĆI" NOSIOCI].
- "VRUĆI" NOSIOCI TIPIČNO UVEĆAVAJU V_{TH} NMOS, A SMANJUJU V_{TH} PMOS FET-a.
- USLED HCE KARAKTERISTIKE MOSFET-a DRIFTUJU TOKOM VREMENA [MANJA POUZDANOST]
- HCE KARAKTERISTIČAN ZA KRATAK KANAL [ISPOD 1μm].

D CMOS LATCH-UP EFFECT

CMOS SCR - [SILICON CONTROLLED RECTIFIER (TIRISTOR)]

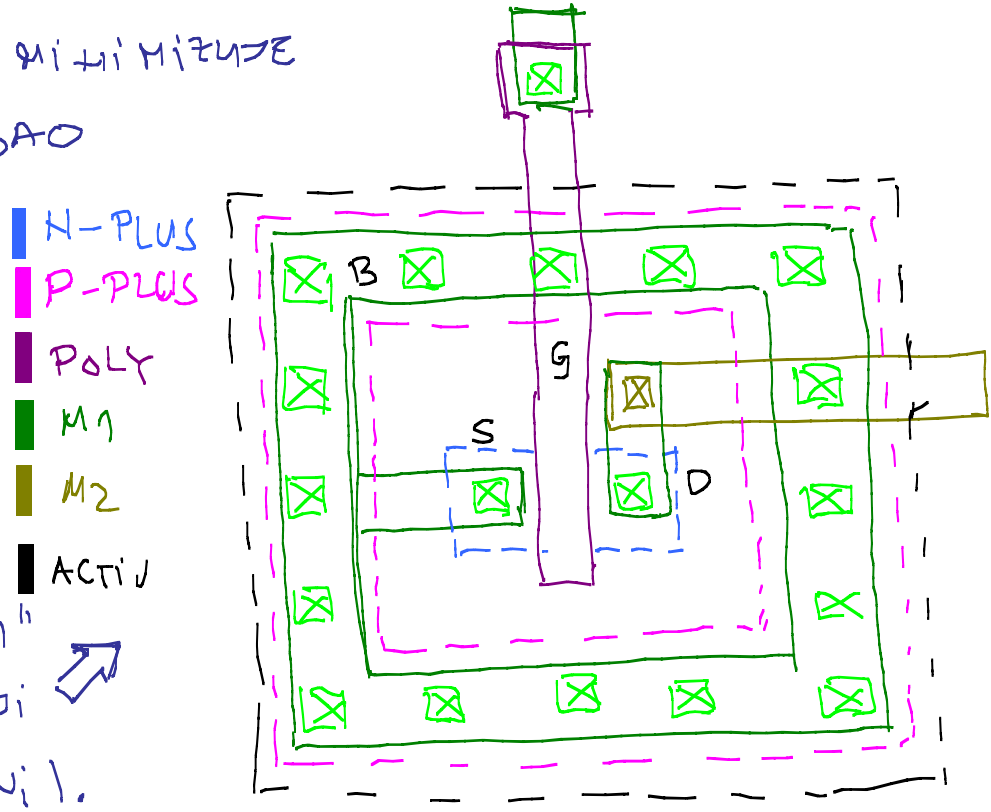




- UKOLIKO SCR PROVEDE DOLAZI DO KRATKOG SPOJA IZMEĐU MASE I NAPAJANJA KOJI NAJČEŠĆE DOVODI DO UNIŠTENJA CELOG IC-a!

(U NAJBOLJEM SLUČAJU IC SE MOŽE OPORAVITI RESTARTIRANJEM NAPAJANJA)

- ZADATAK PROJEKTANTA IC-a JE DA MINIMIZUJE R_{nwell} i R_{psubs} KAKO BI SE IZBEGAO LATCH-UP EFEKAT.
- ZA MINIMIZACIJU $\{R_{nwell}, R_{psubs}\}$ ŠTO VIŠE WELL i BULK KONTAKATA.
- TRANZISTORI KOJI NOSE VELIKE STRUJE (IO ĆELIJE) TREBA DA BUDU OPASANI "ZAŠTITNIM PRSTENOM" [GUARD-RING] KOJI SE OBIČNO SASTOJI OD KONTAKATA PREMA SUPSTRATU (SUPSTRATU).



SPICE MODEL MOS-FETa

- LEVEL 1 [SCHICMAN-HODGES] SQUARE-LOW, LONG CHANNEL. NE UZIMA U OBZIR EFEKTE KRATKOG KANALA. BAZIRA SE NA I-V KARAKTERISTICAMA (PRETHODNO IZVEDENI IZRAZI ZA STRUJE). OVO JE NAJEDNOSTAVNIJI MODEL.

- LEVEL 2. BAZIRA SE NA GEOMETRIJI MOS STRUKTURE I FIZICI POLUPROVODNIKA (INTEGRO-DIFERENCIJALNE JEDNAČINE). UZIMA U OBZIR EFEKTE KRATKOG KANALA [LIBL, DIBL, V_{sat}, $\mu_{n,eff}$, ...]. NAŽALOST, UZIMANJE U OBZIR 3D-EFEKATA U SUB-MIKRONSKIM PROCESIMA NA ČISTO FIZIČKOM NIVOU REZULTUJE SUVIŠE KOMPLIKOVANIM MODELOM KOJI JE NEEFIKASAN SA STANOVIŠTA SIMULACIJE KOLA.

- LEVEL 3. POLU-EMPIRIJSKI MODEL KOJI SE BAZIRA NA KOMBINACIJI ANALIZE I MERENJA. [FITOVANJE]. SVI SAVREMENI CMOS PROCESI (ISPOD 1 μm) KORISTE OVAJ TIP MODELA. U INDUSTRIJI NAJZASTUPLJENIJI BSIM.

  - BSIM [BERKELEY SHORT-CHANNEL INSULATED GATE FET MODEL] IMA OKO 200 PARAMETARA (VERZIJA BSIM3V3) I OBIČNO SE OZNAČAVA SA "LEVEL 49".

Table 3.6 BSIM3-V3 model parameter categories, and some important parameters.

Parameter Category	Description
Control	Selection of level and models for mobility, capacitance, and noise LEVEL, MOBMOD, CAPMOD
DC	Parameters for threshold and current calculations VTH0, K1, U0, VSAT, RSH,
AC & Capacitance	Parameters for capacitance computations CGS(D)O, CJ, MJ, CJSW, MJSW
dW and dL	Derivation of effective channel length and width
Process	Process parameters such as oxide thickness and doping concentrations TOX, XJ, GAMMA1, NCH, NSUB
Temperature	Nominal temperature and temperature coefficients for various device parameters TNOM
Bin	Bounds on device dimensions for which model is valid LMIN, LMAX, WMIN, WMAX
Flicker Noise	Noise model parameters

DA BI SE UZELI U OBZIR PARAZITNI EFEKTI NEOPHODNO JE NAVESTI PARAMETRE IZ TABELE 3.7 PRILIKOM INSTANCIRANJA MOS-FET TRANZISTORA U SPICE NETLISTU [SPICE IH DIFOLTNO NE UZIMA U OBZIR ?.].

Table 3.7 SPICE transistor parameters.

Parameter Name	Symbol	SPICE Name	Units	Default Value
Drawn Length	*L*	L	m	–
Effective Width	*W*	W	m	–
Source Area	*AREA*	AS	m^2	0
Drain Area	*AREA*	AD	m^2	0
Source Perimeter	*PERIM*	PS	m	0
Drain Perimeter	*PERIM*	PD	m	0
Squares of Source Diffusion		NRS	–	1
Squares of Drain Diffusion		NRD	–	1

□ PVT [PROCESS VOLTAGE TEMPERATURE] VARIATIONS

VARIJACIJE PROCESA SE MOGU KLASIFIKOVATI KAO: VARIJACIJE PROCESNIH PARAMETARA I VARIJACIJE DIMENZIJA KOMPONENTE.

▷ VARIJACIJE PROCESNIH PARAMETARA: KONCENTRACIJA PRIMESA (N_A, N_D), DEBLJINA OKSIDA (t_{ox}), DUBINA DIFUZIJE (x_j). REZULTUJU DIVERGENCIJOM $R_\square$ i PARAMETARA TRANZISTORA (npr. V_{TH}).

▷ VARIJACIJE DIMENZIJA KOMPONENTE SU UZROKOVANE KONAČNOM REZOLUCIJOM FOTOLITOGRAFSKOG PROCESA. REZULTUJU DIVERGENCIJOM ODNOSA (W/L) i ŠIRINE VEZA (POLY, METAL).

VEĆINA VARIJACIJA JE NEKORELISANA POŠTO OBIČNO NASTAJE U RAZLIČITIM KORACIMA PROIZVODNJE. npr. VARIJACIJA DUŽINE KANALA (POLY DEPOSITION STEP) NIJE U KORELACIJI SA VARIJACIJOM NAPONA PRAGA (CMP i V_{TH} IMPLANTACIONI STEPI).

- VARIJACIJA NAPONA PRAGA $(V_{TH}) = f(t_{ox}, N_{SUB}$, POVRŠINSKA STANJA (NAELEKTRISANJA),...) RANIJE δV_{TH} i DO 50 %, DANAS (SAVREMENI PROCESI) $\Delta V_{TH} \simeq 25 \div 50$ mV.
- VARIJACIJE $k_n = f(t_{ox}, \mu_{n,eff})$.
- VARIJACIJE $(W; L) = f$(REZOLUCIJA FOTOLITOGRAFSKOG PROCESA). VARIJACIJA W NASTAJE U STI/FOX KORAKU, A VARIJACIJA L U KORAKU DEPOZICIJE POLY GEJTA. ⇒ VARIJACIJA W NIJE U KORELACIJI SA VARIJACIJOM L.

□ DFM (DESIGN FOR MANUFACTURABILITY)

- INFORMACIJE O VARIJACIJAMA PROCESA SE DAJU KROZ ODGOVARAJUĆE SPICE MODELE: PVT KORNERI (FF, SS, TT, FS, SF, FT, ST, TF, TS) GDE JE F-FAST, T-TYPICAL I S-SLOW I PRVO SLOVO ZA NMOS, A DRUGO ZA PMOS. NPR. FS PREDSTAVLJA KOMBINACIJU BRZOG NMOS I SPOROG PMOS TRANZISTORA.

- MONTE-CARLO ANALIZOM (SIMULACIJOM), GDE SE PARAMETRI KOMPONENTE/PROCESA MENJAJU PO SLUČAJNOM ZAKONU, MOŽE SE DOĆI DO DISTRIBUCIJE PARAMETARA PERFORMANSI KOLA.

- "UMETNOST" DFM-a JE PRONAĆI OPTIMALNE PARAMETRE PROCESA I DIMENZIJA TAKO DA VISOK PROCENAT (>98%) PROIZVEDENIH KOLA ISPUNI ZAHTEVE PO PITANJU PERFORMANSI ZA ŠTO JE MOGUĆE MANJU POVRŠINU.

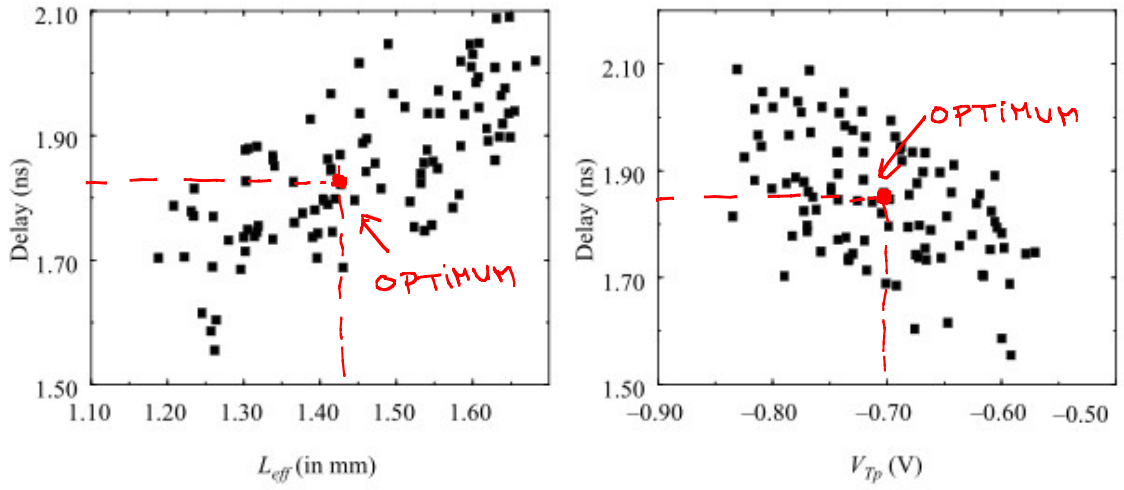
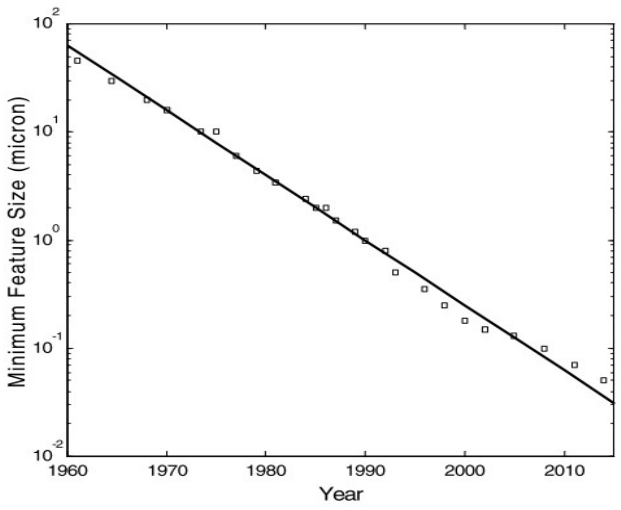


Figure 3.38 Distribution plots of speed of adder circuit as a function of varying device parameters, as obtained by a Monte Carlo analysis. The circuit is implemented in a 2 µm (nominal) CMOS technology (*courtesy of Eric Boskin, UCB, and ATMEL corp.*).

SKALIRANJE



→ REDUKCIJA MINIMALNE DIMENZIJE ≈ 2 PUTA / 5 GODINA. CILJ JE DA SE SA SVAKIM NOVIM PROCESOM DOBIJE DUPLO MANJA POVRŠINA ZA ISTU FUNKCIONALNOST (ILI DUPLO VIŠE FUNKCIONALNOSTI ZA ISTU POVRŠINU). NPR. AKO JE INICIJALNI PROCES SA MINIMALNOM DIMENZIJOM $L_{min} = 1\,\mu m$ PROCES NOVE GENERACIJE BI TREBALO DA IMA MINIMALNU DIMENZIJU PRIBLIŽNO $\sqrt{\frac{L_{min}^2}{2}} = \frac{L_{min}}{\sqrt{2}} \approx 0.7\,\mu m$.

Table 3.8 Scaling scenarios for short-channel devices.

Parameter	Relation	Full Scaling	General Scaling	Fixed-Voltage Scaling
W, L, t_{ox}		$1/S$	$1/S$	$1/S$
V_{DD}, V_T		$1/S$	$1/U$	1
N_{SUB}	V/W_{depl}^2	S	S^2/U	S^2
Area/Device	WL	$1/S^2$	$1/S^2$	$1/S^2$
C_{ox}	$1/t_{ox}$	S	S	S
C_{gate}	$C_{ox}WL$	$1/S$	$1/S$	$1/S$
k_n, k_p	$C_{ox}W/L$	S	S	S
I_{sat}	$C_{ox}WV$	$1/S$	$1/U$	1
Current Density	$I_{sat}/Area$	S	S^2/U	S^2
Ron	V/I_{sat}	1	1	1
Intrinsic Delay	$R_{on}C_{gate}$	$1/S$	$1/S$	$1/S$
P	$I_{sat}V$	$1/S^2$	$1/U^2$	1
Power Density	$P/Area$	1	S^2/U^2	S^2

→ POTPUNO SKALIRANJE [FULL-SCALING] PODRAZUMEVA DA SE SVE DIMENZIJE I NAPONI (V_{DD}, V_{TH}) SKALIRAJU ISTIM FAKTOROM (S), GDE JE ($S > 1$). NA OVAJ NAČIN ELEKTRIČNO POLJE OSTAJE NEPROMENJENO ($E \propto V/x$, CONSTANT FIELD SCALING) OVAJ KONCEPT JE VIŠE TEORIJSKI I TEŠKO SE OSTVARUJE U PRAKSI.

→ SKALIRANJE SA KONSTANTNIM NAPONOM [FIXED-VOLTAGE SCALING]. OVDE SE SVE DIMENZIJE SKALIRAJU FAKTOROM (S) DOK NAPONI OSTAJU NEPROMENJENI. MOTIV ZA OVAJ TIP SKALIRANJA JE U TOME ŠTO NIJE PRAKTIČNO SKALIRATI NAPON NAPAJANJA SA SVAKIM NOVIM PROCESOM JER SE NA TAJ NAČIN GUBI KOMPATIBILNOST PO PITANJU LOGIČKIH NIVOA. ZA SUB-MIKRONSKE PROCESE OVAJ KONCEPT JE TEORIJSKI. ($V = const$, $x \to \frac{x}{S} \Rightarrow E \propto \frac{V}{x} \uparrow$ ZA $S > 1$) PRAKTIČNO, ZA $E > E_C$ NE DOBIJA SE

POBOLJŠANJE PERFORMANSI (ZASIĆENJE BRZINE NOSILACA), A PRI TOME POTROŠNJA OSTAJE ISTA, D GENERALNO SKALIRANJE [GENERAL SCALING]. PODRAZUMEVA DA SE DIMENZIJE SKALIRAJU FAKTOROM (S), A NAPONI FAKTOROM (U) GDE JE ($S \neq U$). OVO JE KOMPROMISNA TEHNIKA IZMEĐU FULL-SCALING (CONSTANT-FIELD) i FIXED-VOLTAGE KONCEPTA. PRAKTIČNO, SVI SAVREMENI PROCESI KORISTE OVAJ PRISTUP.

FIZIČKA GRANICA SKALIRANJA NAPONA JE:

- NAPON KOJI ODGOVARA ENERGETSKOM PROCEPU Si (BANDGAP VOLTAGE, $V_{BS(Si)} \approx 1.12$ V) SE NE MOŽE SKALIRATI.
- ZA VRLO MALE VREDNOSTI V_{TH} (NPR. ISPOD NEKOLIKO $V_T = kT/2$) NE MOŽE SE POTPUNO ISKLJUČITI TRANZISTOR. POREĐ TOGA, UTICAJ PVT VARIJACIJA NA KARAKTERISTIKE PROJEKTOVANOG KOLA POSTAJE DOMINANTAN.

Table 3.9 MOSFET technology projection for high performance logic (from [SIA01]).

Year of Introduction	2001	2003	2005	2007	2010	2013	2016
Drawn channel length (nm)	90	65	45	35	25	18	13
Physical channel length (nm)	65	45	32	25	18	13	9
Gate oxide (nm)	2.3	2.0	1.9	1.4	1.2	1.0	0.9
V_{DD} (V)	1.2	1.0	0.9	0.7	0.6	0.5	0.4
NMOS I_{Dsat} (μA/μm)	900	900	900	900	1200	1500	1500
NMOS I_{leak} (μA/μm)	0.01	0.07	0.3	1	3	7	10

- DA BI SE POVEĆALA GUSTINA PAKOVANJA U SUB-SUB-MIKRONSKIM (NANO) TEHNOLOŠKIM PROCESIMA (ISPOD 65nm) KORISTE SE 3D MOS STRUKTURE POPUT FinFETa i VFETa (VERTICAL FET). PROBLEM KOD OVOG KONCEPTA JE ŠTO JE POSTUPAK PROIZVODNJE IC-a SA OVAKVIM KOMPONENTAMA ZNAČAJNO SKUPLJI OD KLASIČNOG (PLANARNOG) POSTUPKA (NEPRISTUPAČAN MATLIM, START-UP, KOMPANIJAMA) TAKO DA JE PROIZVODNJA IC-a U OVIM PROCESIMA UGL. EKSKLUZIVA DOSTUPNA VELIKIM KORPORACIJAMA (Apple, SAMSUNG, MICROSOFT, Google, ...) I VRHUNSKIM UNIVERZITETSKIM/ISTRAŽIVAČKIM CENTRIMA.

→ "PERCE"

FinFET [BERKELEY]

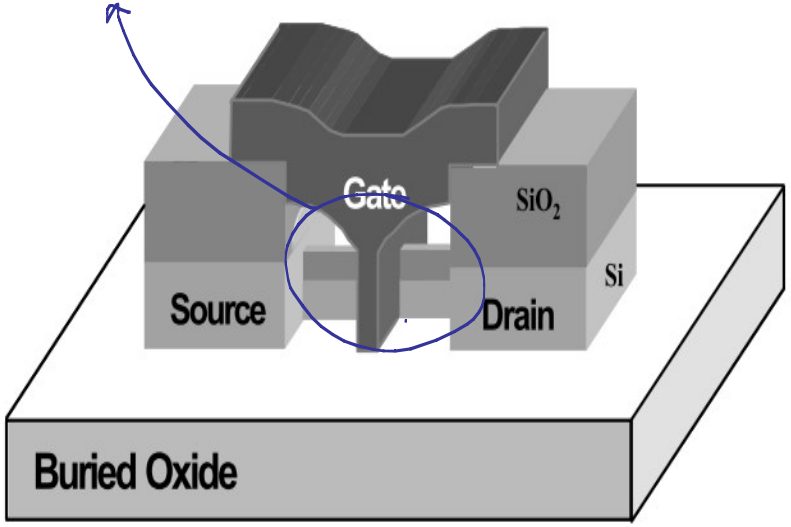


Figure 3.41 FinFET dual-gated transistor with 25 nm channel length [Hu99].

VFET [Eaglesham00]

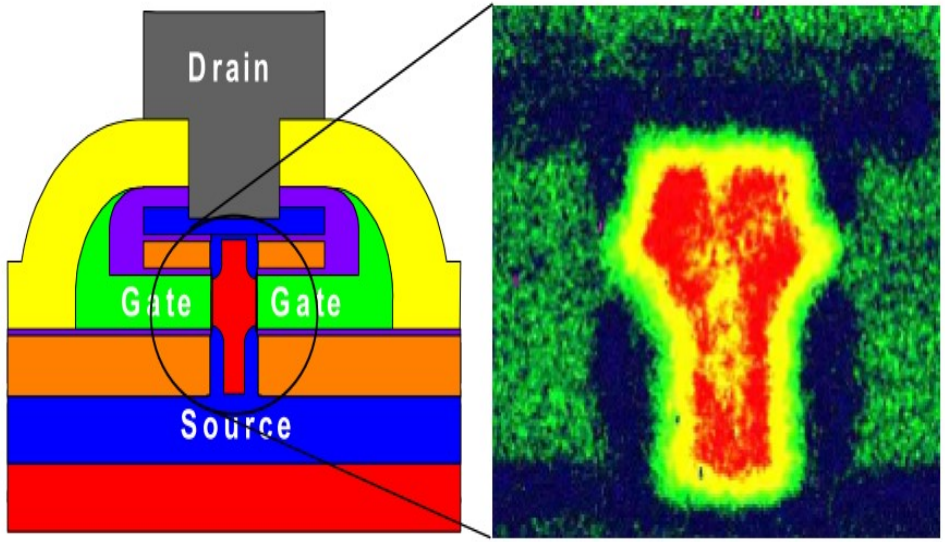


Figure 3.42 Vertical transistor with dual gates. The photo on the right shows an enlarged view of the channel area.